



VHF

communications

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*A Publication
for the Radio-Amateur
Especially Covering VHF,
UHF and Microwaves*

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*Home-made
high-quality
attenuators*



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Especially Covering VHF, UHF, and Microwaves

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With deepest sorrow we announce the death of the revered owner and head of our company, who was torn from our midst by a tragic accident.

Terry D. Bittan
G 3 JVQ, DJ Ø BQ

We will greatly miss the enormous activity, care and scope of his ideas, and will strive to continue his work in his sense.

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Terry D. Bittan
– The Staff –

Baiersdorf, the 17th of March 1985

We can only hope that you – our readers – will accept our apology for the excessively late appearance of this edition. The reason is the tragic death of Terry D. Bittan by an airplane accident. We are trying hard now to work with a couple of translators (radio amateurs with engineering background and with fluent German). Although it is very difficult to fill the big gap Terry left behind, we will continue with VHF COMMUNICATIONS. May we ask you for some patience with regard to variations in future translations and to appearance dates ?

Thank you.

Robert E. Lentz, DL 3 WR



Carsten Vieland, DJ 4 GC

Compact BNC Attenuators

Many radio amateurs dislike the idea to attenuate some receive, transmit or oscillator signals. On the other hand, attenuation is very important in RF-measuring technology. The following article is to describe how compact, and mechanically robust attenuators can be constructed with amateur means that have the highest possible cutoff frequency, and li-

near phase transmission characteristics. It is true, a lathe is necessary to construct the described attenuators, however, the author is to also show methods that allow one to carry out one's own experiments easily.

Figure 1 shows the attenuators manufactured by the author with values of 3, 6, 10, 20, and 40 dB.



Fig. 1: A series of compact BNC-attenuators

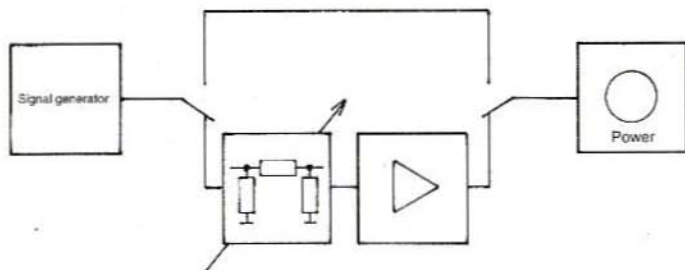


Fig. 2:
The amount of the gain is of
the same value as the selected
attenuation

1. APPLICATIONS

With the aid of a (variable) attenuator, it is possible to measure the gain of, for instance, a preamplifier or low-power amplifier by compensation (see Figure 2).

Mismatched signal sources and consumers in a 50 Ω system will cause standing waves with voltage and current maxima. Gain comparisons of antennas (with the aid of a mismatched receiver) or RF-voltage measurements, will not provide true values. It is, however, possible to obtain a forced matching to the line impedance with the aid of attenuators, at least to avoid the greatest errors (Figure 3).

Many signal sources such as noise diodes have source impedances that are far from that of the real 50 Ω . For instance, the noise source described by DC8UG in Edition 3/1984, which uses a diode BAT 31, has a source impedance of a few

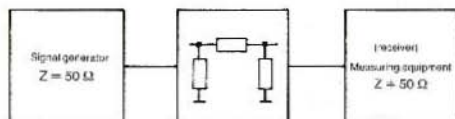


Fig. 3: Forced matching of a signal source

ohms. A consumer that is not ideally matched will reflect a portion of the noise power, which is once again reflected from the mismatched signal source and will cause standing waves on the interconnection line between source and consumer.

As a result of the frequency dependence of the current/voltage distribution, this will result in a selective fading on the line with considerable errors with respect to the actual amount of the signal power. When carrying out a forced matching to 50 Ω with the aid of an attenuator, it is also possible for the signal power to be reduced to a handy value with the aid of the attenuator. Of course, it is necessary for the attenuator used to possess a high return loss and constant transfer behaviour over the whole frequency range in question.

The return loss from the end of an open, or shorted attenuator is twice as high as its attenuation value since the reflection must pass through the resistor network twice. A fixed attenuation of 10 dB is usually sufficient to obtain reliable conditions.

The alignment of highpass, lowpass or bandpass filters should also be made under controlled and reproducible conditions. Mismatched generators and detectors transform reactances into the filter. These will simulate frequency shifts or ripple which will change considerably on only replacing a connection cable.

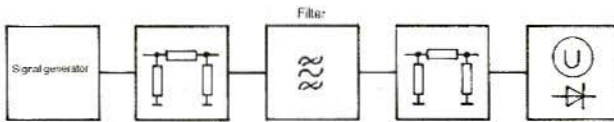


Fig. 4:
Measuring setup for
measuring a filter curve

In order to measure the "real" transmission characteristics of, for instance, an interdigital filter, or a selective amplifier, it is necessary for the input and output of this stage to be provided with matching attenuators, (10 dB) as shown in **Figure 4**. The use of a high-quality wideband detector (thermal power meter) can replace the output attenuator. When using such attenuators, far less demands are placed on the impedance behaviour of the signal source and the detector.

Many simple, free running signal generators will show considerable feedback on the oscillator frequency when connecting a selective consumer. Extensive discriminator effects will be noticed on measurements on antennas, filters, or resonant amplifiers, which will then show frequency shifts, or notches. A 10 dB attenuator, possibly using a subsequent wideband amplifier (DJ7VY) will be of great help. The reverse transmission of such an amplifier itself is usually not sufficient.

2. ATTENUATORS AVAILABLE ON THE MARKET

Various manufacturers offer precision attenuators with N, SMA, or APC 7 connectors. These attenuators not only offer excellent electrical characteristics but also exorbitant prices.

"Low-cost" attenuators with BNC-connectors are available from approximately 50,- DM upwards. The resistor combination is made from mass resistances and will show a noticeable reflection even at 1 GHz.

Switchable attenuators up to 1 GHz (2 GHz) with steps of 0.1 dB, 1 dB, and 10 dB are available for approximately 500,- DM, each (Texscan). Especially of interest are high-power attenuators of up

to 250 W in stripline technology that are able to operate up to 2 GHz. However, a careful construction (with heat sink) must be made here. Such an attenuator allows one, for instance, to examine the harmonic spectrum of a transmitter with the correct amplitude.

Less expensive are the RF-potentiometers manufactured by Preh. The advantage is the high maximum attenuation of more than 100 dB. This disadvantage is an insertion loss of approximately 2 dB, as well as a varying linearity. Especially at low impedances, the impedance is not constant. In excess of approximately 100 MHz, couplings appear between input and output which means that the maximum attenuation value deteriorates.

It is possible in the high-power range to use rings of cable that have been previously measured. It should be noted that the attenuation is strongly frequency-dependent and it has been seen that this increases with time, especially when using cheaper cables.

3. DESIGN CRITERIA FOR CONSTRUCTION

When constructing attenuators, one should try to achieve the highest possible upper cutoff frequency, since this will also increase the accuracy of measurements at lower frequencies. Experiments with coaxial construction can often not be realized due to the difficulty of obtaining the required resistors. It is not only necessary to obtain the correct resistance value, but its geometry will also have an effect on the cutoff frequency of the attenuator. Disk-type resistors are required for the grounded resistors in a coaxial system.

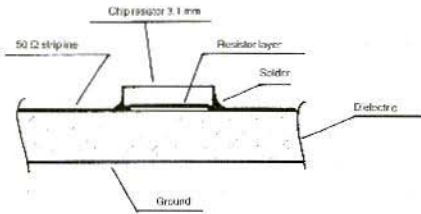


Fig. 5: Construction principle of a chip resistor

Stripline technology results in less problems. In this case, chip resistors can be soldered onto the conductor side of a board.

According to (2), a frequency dependence will occur with any type of resistors when the length of the component is greater than $5/1000$ of the wavelength of the signal in question. Regarding this, the 3.1 mm long chips would be suitable up to the 70 cm band. When using axial, non-helical 0.5 W-resistors, a frequency of approximately 100 MHz should be achievable.

A higher, upper cutoff frequency can mainly be realized with the aid of an impedance-optimized construction of the resistor/stripline combination (Figure 5). The first approximations of the resistor path are the same impedance relationships as in the case of striplines.

Experiments made by cutting the board and by di-

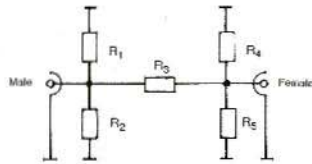


Fig. 6: The resistances to ground are distributed; values in Table 1

rectly soldering the chips to the lower side of the board in order to comply with the reducing of the impedance along the resistance towards ground, did not bring any improvement.

Round resistors are unfavorable due to the low amount of capacitance. In addition, a frequency-dependent skin effect is noticed in the direction of the opposite conductor (ground), which greatly increases the actual resistance value. Their use in conjunction with a stripline is not advisable.

From an electrical standpoint, such materials are especially suitable as substrate by which an impedance of 50Ω is achieved with the width of the chip resistor of 1.6 mm. This is the case with 0.8 mm thick epoxy, or 0.5 mm thick RT/duroid substrates. However, the mechanical stability is not sufficient when using board materials in the recommended construction, and for this reason, the author has selected the wellknown 1.5 mm thick,

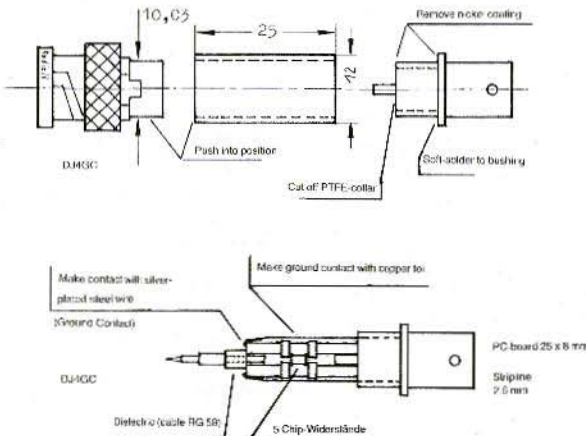


Fig. 7: Construction of an attenuator as shown in Figure 6



double-coated epoxy material. The moderate dielectric quality of this material is not so important due to the non-resonant conductor lane.

The balanced construction using two resistors to ground, as shown in **Figure 6**, causes a reduction of the inductive components and an increase of the power rating. The nominal power rating amounts to 0.5 W. Continuous tests with more than one Watt did not result in any failures.

In order to reduce any capacitive coupling, the 40 dB attenuator comprises two Pi-circuits of 20 dB, each. Since chip resistors are only available in standard values from E 24, it is necessary for small deviations from the flat attenuation value, or nominal impedance, to be accepted (see Table 1).

Attenuation	R ₁	R ₂	R ₃	R ₄	R ₅
3 dB	560	560	18	560	560
6 dB	300	300	39	300	300
10 dB	180	220	68	180	220
20 dB	120	120	240	120	120
40 dB 2x	120	120	240	120	120

Table 1

4. MECHANICAL CONSTRUCTION

A BNC male connector can be screwed onto the thread of the corresponding female connector and then be inserted into a lathe. The turned shaft of the BNC male connector is approximately 3/100 mm thicker than the inner conductor of the brass collar. Both parts are pressed together with the aid of a vice, since the male connector cannot be soldered due to its rubber seal.

The nickel surface of the female connector is turned with the aid of the lathe so that it can be soldered. Firstly solder the completed PC-board to the female connector, after which the connector and the brass collar are soft-soldered together with the aid of a gas burner at moderate pressure. Any residual solder can be easily removed with the aid of the lathe.

Finally, the intermediate brass piece is polished with the aid of emery cloth or steel wool and protected against corrosion with the aid of a clear, metal lacquer. The attenuators can be marked with the attenuation value as shown in Figure 1. Further details can be seen in **Figure 7** and **Figure 8**.

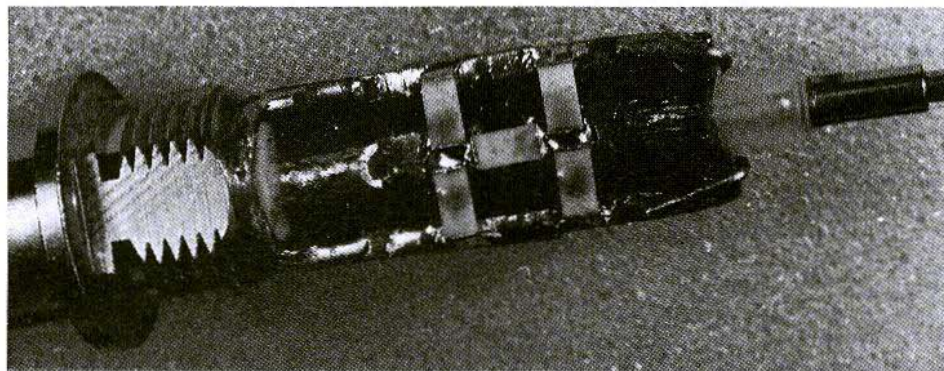


Fig. 8: The 5 chip resistors can be seen as bright rectangles

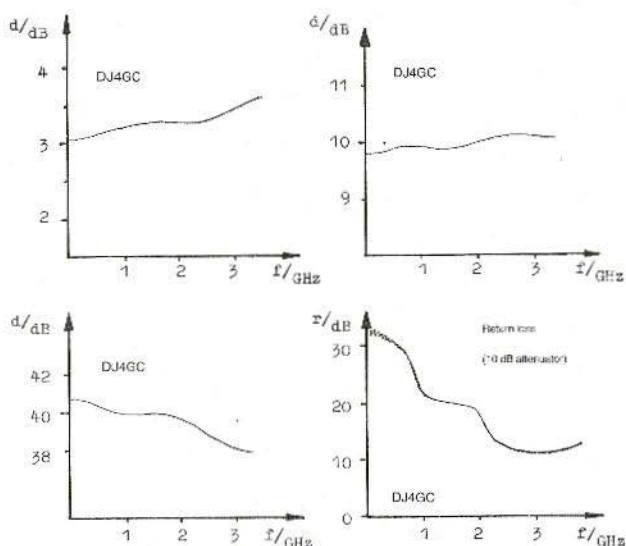


Fig. 9:
Typical transmission and
return loss values

5. MEASURED VALUES

It is interesting to know that it is not easy to measure RF-components equipped with BNC-connectors. The available transmission and reflection measurements show, it is true, the same tendency, with deviations in detail, which are caused by the difference in the adapters from N, or APC 7 to BNC. The poor name of BNC-connectors is unwarranted, and it is firstly due to low-quality products, and secondly due to the fact that no network analyzer or impulse reflectometer are able to work with BNC directly, but only with the aid of one or multiple adapters.

The transmission and reflection characteristics given in **Figure 9** represent the mean values of various measuring setups. The transmission values coincide with the author's measurements made with the aid of a thermal power meter. The slight attenuation reduction of the 20 dB and the 40 dB attenuator at high frequencies is due to capacitive coupling on the board.

The measured values allow unlimited usability up

to the 23 cm band. In the case of the 13 cm and 9 cm bands, the absolute attenuation is still very good, however, the reduced return loss indicates that phase shift occurs due to reactive components. The other diagrams that have not been published show similar characteristics. These compact, and mechanically robust attenuators have proved themselves well in practice.

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UHF-Unterlage Teil 1/2
Kapitel B1



Bernd Bartkowiak, DK 1 VA

A low-noise METEOSAT Converter with GaAs-FET Preamplifier and Mixer Stage

This article is to describe a low-noise microwave converter equipped with GaAs-FETs and designed for reception of the geostationary weather satellite METEOSAT 2 (1691.0 and 1694.5 MHz) or GOES (1694.5 MHz).

Both, circuitry and components were matched to the state-of-the-art. This means that it is possible with only one stable GaAs-FET preamplifier and an optimized GaAs-FET mixer stage to achieve such good technical data that the converter will provide noise-free images without employing additional preamplifiers, and even in the case of small parabolic antennas being used (diameter of the parabolic dish 90 cm).

A feeding possibility for the converter (channel 1) via the IF-cable, as well as for a possibly employed preamplifier has been provided for. The converter is accommodated in a tin-metal case and may be incorporated in a weatherproof macrolon housing for outdoor mounting purposes. This UV-resistant, plastic housing has been provided with a temperature-dependent heating which prevents the converter from being damaged by condensed water. This also avoids a "freezing" of the converter during winter-time operation.

A home-made construction of this converter is, however, recommended only to those experienced UHF-SHF amateurs who have access to at least a minimum of measuring equipment (fre-

quency counter, multimeter). The complete construction can be carried out within approximately three to four hours. The assembly is limited to soldering activities, while mechanical work will not be required, since the PC-board is being supplied with the holes already drilled, and the housing already punched.

Supplementary to the kit, a set of parts for outdoor mounting is available for supply, which comprises a macrolon housing with the holes already drilled, and a temperature-controlled heating. **Figure 1** shows the built-in converter.

1. TECHNICAL DATA

The following values were measured at the converters, designed according to **Figure 2**:

Input frequency channel 1:	1694.5 MHz
channel 2:	1691.0 MHz
Intermediate frequency:	137.5 MHz
Noise figure F:	typ. 1.8 dB
Insertion gain:	typ. 26 dB
Operating voltage (intern. stab.)	12 - 15 V
Operating current without heating	typ. 100 mA
with heating	typ. 350 mA
Connect. standard:	N
Impedances:	50 Ω

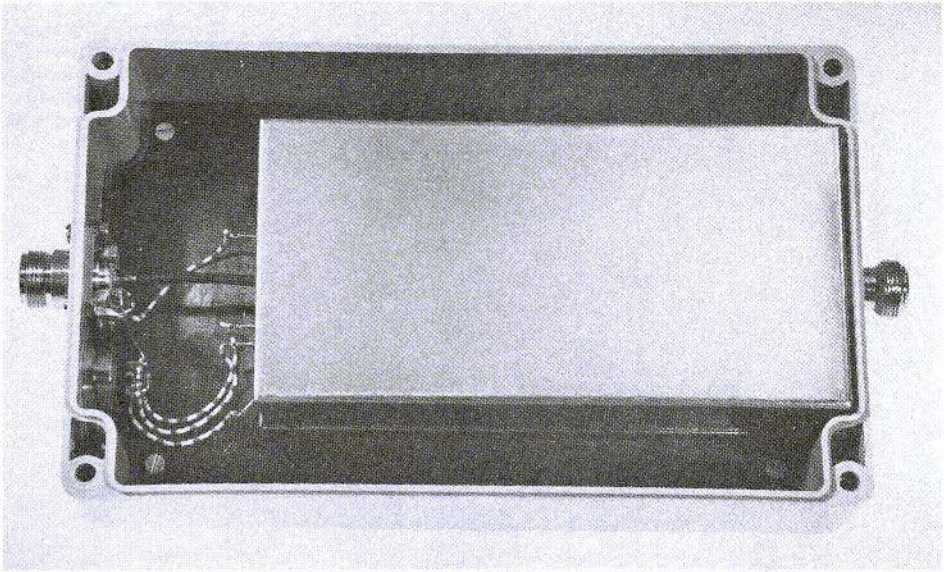


Fig. 1: Ready-to-operate METEOSAT converter in plastic box

2. CIRCUITRY

Microwave converters using stripline technology are replacing the well-known and widely spread finger-filter converters. The disadvantages of the

finger-filter converters, i.e. their expensive mechanical design and their somewhat obsolete technical data can be avoided by the construction of a METEOSAT converter in stripline technology which is to be described in the following.

In comparison with the finger-filter converter, the printed image-frequency filter has a considerably

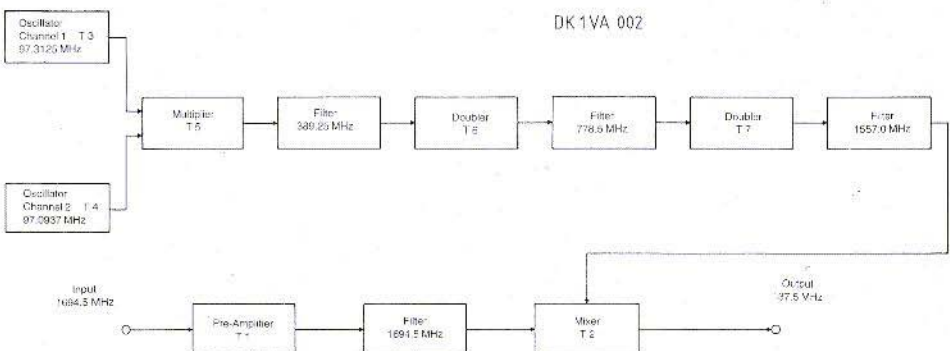


Fig. 2: The frequencies shown in the block diagram apply to operation on METEOSAT Channel 1



lower Q which, at least in part, can be compensated for by appropriate measures:

The somewhat higher insertion loss of the filter (approx. 2 dB) will be completely compensated for on the preamplifier side by a higher gain, and on the mixer side by a lower mixer noise figure. What remains is the wider bandpass curve of the stripline filter, which, however, is still narrow enough to suppress the undesired image frequency by more than 20 dB.

With regard to a good single-sideband noise figure, a higher attenuation of the image frequency is not required.

Most valuable, however, is a stable GaAs-FET preamplifier stage which, even at narrowband antenna drive elements, does not show any tendency to oscillation, and nevertheless exhibits a good noise figure.

The METEOSAT converter constructed according to **Figure 3**, widely exploits the possibilities of modern GaAs-FET technology. The favorable total noise figure of only 1.8 dB, as well as the high insertion gain of more than 25 dB, provided on a comparatively small PC-board, prove this significantly.

Also to be mentioned here is the injection frequency portion provided with a consequent bandpass filter coupling, which offers to the mixer a crystal-stabilized, low-spurious oscillator signal with an output of 3 dBm and a spurious rejection of approx. -45 dB. Due to the built-in voltage regulators, the electrical parameters of the converter are virtually independent of the operating voltage. A minimum voltage of 12 V, however, must not be dropped below.

It is possible for the converter to be supplied with the operating voltage via the IF-line (137.5 MHz) on channel 1. In turn, a possibly employed GaAs-FET preamplifier will be fed remotely from the converter. The facilities required for this purpose have already been provided on the PC-board.

For an outdoor mounting of the unit directly at the antenna, it is necessary for protective measures to be taken. For this purpose, the converter will be incorporated into a waterproof, UV-resistant macrolon housing which can be used over a wide

temperature range. The built-in heating (5 W resistor), being activated via a temperature-controlled switch from approx. 10°C on, reliably prevents the formation of condensed water. In conjunction herewith, also the drifting of the oscillator due to heavy temperature fluctuations, will be reduced to a reasonable level.

3. COMPONENTS

T 1, T 2:	CFY 19, CFY 14, MWT 11, MGF 1202, MGF 1400 or similar
T 3, T 4:	U 310 (Siliconix)
T 5 - T 7:	BFR90A (Philips)
D 1 - D 3:	1 N 4001
2 x 78L09	
C 1 - C 9:	Mini trimmer 5 pF (green) SKY
C 10, C 11:	dito 10 pF (black) SKY
C 13, C 22, C 23:	10 pF trapezoid (Stettner)
C 14:	47 pF trapezoid (Stettner)
C 12, C 15:	Stripline chip capacitor 100 pF - 1 nF (ATC)

All capacitors, not designated:

Ceramic type 470 - 1500 pF

L 5 - L 7: Neosid 5061 (blue/brown)

4 pcs. 1 μ H chokes, spacing 7.5 mm, Jahre, Neosid and others

2 x 1 μ F/35 V tantalum electrolytic

N-flange sockets with BNC flange (flat!)

Crystals: 97.0937/97.3125 MHz, 5th harmonic, HC-43/U

Trimmer resistor: 100 Ω , spacing 10/5 mm

2 x ferrite beads, 1.2 mm long

4. CONSTRUCTION HINTS

Starting out from a complete kit with drilled PC-board and punched housing, it is possible for the converter to be completely assembled by experienced VHF-SHF amateurs within three to four hours. With a correct construction, supported by the following detailed mounting instructions, and



with a careful installation of the special components (trapezoid capacitors, semiconductors), the converter should work faultlessly at the first attempt, after alignment has been terminated.

If a spectrum analyzer, a noise figure measuring setup, and a microwave test-signal generator are not available, it is also possible for the alignment to be performed with amateur means, yielding good results. One will require for this purpose a 500 MHz frequency counter, a multimeter, as well as a METEOSAT-signal provided by an antenna.

The double-coated, epoxy PC-board DK1VA 002 whose dimensions are 145 mm x 72 mm, is shown in **Figure 4**. The optimum sequence of locating the components on the board will now be described step by step.

4.1. Converter in Tin-Metal Case

4.1.1. The ground surface of the PC-board should be cleaned with the aid of a cotton ball and some polish (car polish) from the partly ugly stains that may occasionally result from the galvanization process. Now that the PC-board is sparking clean, the remaining polish should be removed with the aid of soap and a little brush.

4.1.2. The N-flange sockets are flatly passed from outside into the 4 mm holes of the tin-metal frame and soldered around the edges after having been positioned in a way, that the edges of the N-sockets are in parallel with the cutting edges of the tin-metal frame.

If, after completed construction, the converter is to be installed in the weatherproof outdoor hou-

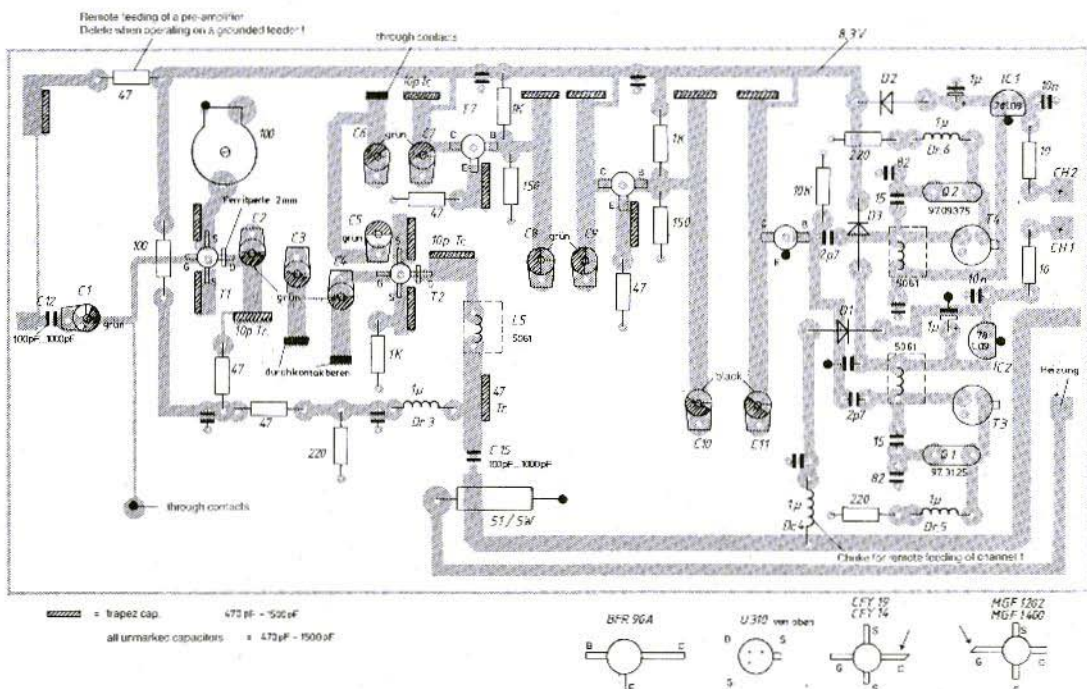


Fig. 4: PC-board DK1VA002 is double coated



sing, the IF-side N-socket must not be soldered on. Later on, one will pass a piece of thin coaxial cable through the 4 mm hole having been provided for this N-socket. The IF N-socket is adjacent to the 3.6 mm holes for the PTFE feedthroughs.

4.1.3. Solder the PC-board into the tin-metal frame.

Solder the case temporarily together at two points and fit in the PC-board. The 50 Ω input and output striplines are located exactly on the pins of the N-sockets (with an assumed mounting in the outdoor housing, the PC-board would lie only on the pin of the input N-socket). The printed islands for the power supply are lying exactly below the corresponding holes for the PTFE feedthroughs. Solder the PC-board tightly into place at one point, and arrange it horizontally in the frame of the housing. Then, solder the PC-board **all around the edges** into the frame.

4.1.4. The "cold" ends of the stripline circuits L 3, L 4, and L 13 are through-contacted to the ground surface by means of copper foil. The foil should be cut approximately as wide as the resonant circuits are. On both sides of the PC-board, the foil must be bent down forming sharp edges, and be subsequently soldered into place. Under no circumstances, the through-contacting will be permitted by means of wires only.

4.1.5. Solder in all trap capacitors. The value is uncritical (470 to 1500 pF). With trap capacitors C 13, C 14, C 22, and C 23, however, the value must strictly be maintained.

Approximately by half their length, the trap capacitors are inserted into the corresponding slots on the PC-board and soldered into place at both sides. The temperature of the soldering iron should not exceed 300°C during this procedure, since otherwise the trap capacitors could crack.

4.1.6. Solder into place all bypass capacitors. They are contained in the component location plan without value indications. The value of these capacitors is uncritical (470 to 1500 pF). It is, however, important for them to be soldered into place as short as possible. One little leg of these capacitors is soldered to the ground surface, the other one to the corresponding conductor lane.

4.1.7. Solder into place the three Neosid filters with brown/blue colour point. Previously, the unconnected third leg of the filter is carefully pulled out of the coil former and the copper ground tags are removed with a sharp edge cutter. Now, place the filter flatly onto the ground surface of the PC-board and solder into place after previous correct arrangement.

4.1.8. Now the remaining capacitors are soldered into place according to the component location plan. Please, pay attention to the values! With the tantalum electrolytics, also pay attention to polarity!

C 12 and C 15 are tiny chip capacitors which are soldered directly to the conductor lanes with the aid of tweezers.

4.1.9. Solder into place all resistors and diodes. With the diodes, please, pay attention to polarity!

4.1.10. Solder into place all trimmer capacitors. The flat connection tag of the trimmer is sharply bent down by 90°, shortened, and soldered to the ground surface after installation. Before soldering in, uniformly arrange the trimmers on the PC-board; C 10 and C 11 possess a higher capacitance, all other trimmers are identical.

4.1.11. Instal the four chokes (approx. 1 μ H).

CAUTION: When sharply bending down the connecting wires, the coil wire might tear! If required, the coils could be wound also by our readers themselves: 15 turns of enamelled copper wire with a diameter of 0.2 mm, on a former of 2 mm dia.

The printed choke Dr 2 is to be through-contacted at the cold end by means of a wire.

4.1.12. Solder into place the 100 Ω potentiometer. One leg is to be soldered to the ground surface. Finally bring wiper into center position.

4.1.13. Now instal the two voltage regulators (as close as possible above the PC-board). The connection sequence is correct, when the regulators are installed, as shown in the component location plan. Their central leg has to be soldered to the ground surface.

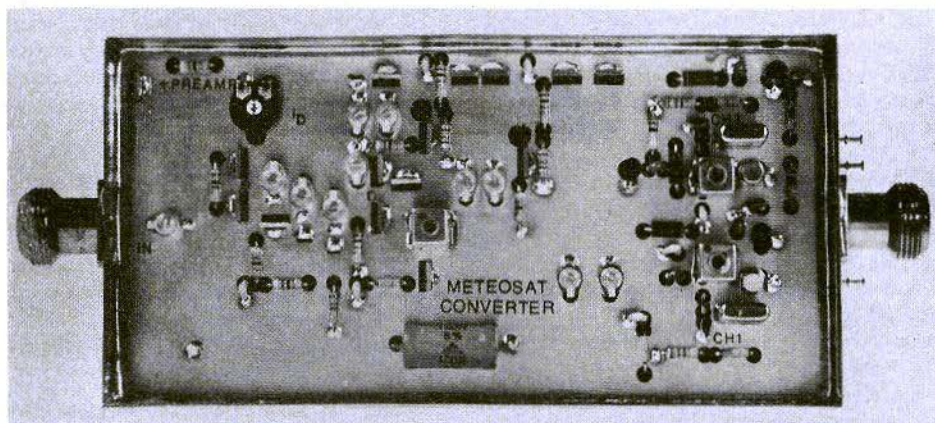


Fig. 5: PC-board ready to align

4.1.14. Solder in the two crystals. They must stand flat on the ground surface. The crystal housing should not be soldered to the ground surface, since this could result in a frequency deviation due to too strong a heating up.

4.1.15. Solder into place the two U 310. The transistors are built in with their nose positioned in accordance with the component location plan. Install both transistors as deep as possible and solder the nose to the ground surface.

4.1.16. Finally install the stripline transistors. The emitter leg of T 5 is bent down by 90° and passed through the PC-board, for which purpose a small notch has previously to be filed. Now the leg is soldered to the ground surface.

The connection legs of the remaining BFR90A are shortened down to 2 mm (previously mark the collector side on the housing). Then the transistors are pushed into the corresponding holes and soldered to the conductor lanes. **CAUTION:** Please, make sure never to mistake base for collector connection!!

For the installation of the GaAs-FETs it is necessary for the usual safety measures to be taken:

The tip of the soldering iron and the tin-metal case must be grounded. Oneself is being discharged by touching the case. Over the drain connection each of T 1 and T 2 a small ferrite bead is passed. Then the FETs are placed into the corresponding holes and soldered into place.

ATTENTION: Usually, with the Mitsubishi GaAs-FETs the pointed little leg is the gate, with Siemens GaAs-FETs, however, it is the drain!!

4.1.17. After the PTFE feedthroughs have been pressed in and soldered into place, the construction can be considered as terminated. The converter should now look like the prototype shown in **Figure 5**.

4.2. Mounting of the Converter in the Weather-proof Outdoor Housing

4.2.1. Instead of the N-socket, an approximately 15 cm long piece of coaxial cable will be soldered onto the IF-output of the converter, (see 4.1.2.). The inner conductor of the coaxial cable is soldered to the 50 Ω stripline of the IF-output, the shielding to ground. **CAUTION:** Solder rapidly, since the dielectric easily melts!

4.2.2. An N-flange socket is passed through from inside to outside and screwed into the front cover of the plastic housing with the aid of M3 screws and nuts. An additionally underlayered M3 solder tag serves as ground point for the shielding mesh of the cable.

4.2.3. Fasten the punched converter-cover onto the pertinax board with the aid of M3 screws and nuts. Install the board into the housing and screw tightly into position. Then press the converter into the cover. Now the N-socket for the antenna input must protrude beyond the housing. The flange of the socket should be in direct contact with the in-

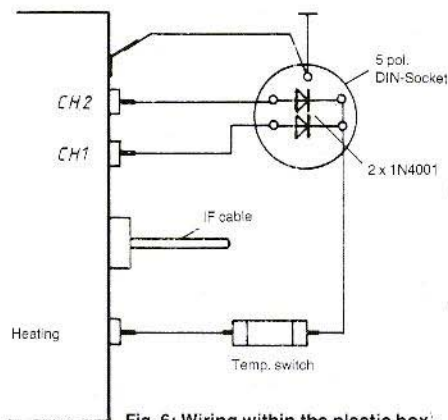


Fig. 6: Wiring within the plastic box

ner side of the plastic housing; to achieve this, the whole converter may be shifted in the longitudinal holes of the cover.

4.2.4. Solder the IF-line to the N-socket; the shielding to the solder tag.

4.2.5. Mount the DIN-socket for the power supply and connect it with the PTFE feedthroughs for channel 1 and 2 with the aid of short lengths of stranded wire. Now the ground line is soldered to the housing. Normally, ground is fed in via the shielding mesh of the coaxial cable.

4.2.6. Instal and connect the thermo switch according to **Figure 6**. CAUTION: The connecting wires of the switch must not be bent with sharp edges, since otherwise the glass body would break!

4.2.7. Before the final mounting, it is necessary for the flanges of the two N-sockets to be coated with silicon rubber, in order to achieve the water tightness required. The bore hole for the N-input socket in the plastic housing must also be made water-tight.

5. HINTS FOR ALIGNMENT

5.1. Eliminate the Sensitivity against the Cover

Before aligning the converter, it is necessary for

the tin-metal cover lying on the conductor lane side (punched cover when mounting in plastic housing) to be coated with a conductive foam material which has to be glued on.

5.2. Bring the 100 Ω potentiometer for the drain current of T 1 into center position.

5.3. Apply the operating voltage to the PTFE feedthrough for channel 1, and measure the current drain of the converter – it should range between 70 and 90 mA.

5.4. Preset all trimmer capacitors, as shown in the component location plan. The final positions of the rotators are **always** in the vicinity of the shown ones. Greater deviations would imply the failure of a component, or a drastic misalignment, e.g. with the multipliers the alignment to a wrong harmonic.

5.5. Measure the voltage at the output of the regulator: approx. 9 V should be present.

5.6. Compare the voltages at the transistors with the values indicated in the circuit diagram. Small deviations are due to transistor spreads and may be neglected; totally different values, however, indicate the failure of a component.

5.7. Measure the voltage at the source resistor of the oscillator transistor T 3 (channel 1) and slowly rotate in the coil core. If the voltage suddenly drops by approx. 0.3 V, the oscillator will be oscillating.

5.8. Measure the voltage at the emitter of T 6 and carefully align trimmers C 11 and C 12 to maximum voltage. Here, a clear maximum must be found. The voltage at the emitter of T 6 increases from approximately 0.4 V with a non-oscillating oscillator (or totally misaligned filter with C 11 and C 12) by approximately 0.3 V to approx. 0.7 V, with the filter optimally aligned.

5.9. Measure the voltage at the emitter of T 7, and align in conjunction herewith the bandpass filter with C 9 and C 11 to maximum voltage. The alignment of these and also of the subsequent circuits must be carried out with sensible care in order to find a clear maximum. The voltage at T 7 should rise by approx. 0.4 to 0.7 V. If the rotator positions of trimmers C 8 to C 11 comply with tho-



se shown in the component location plan, one may go on to the alignment of the mixer.

5.10. Measure the voltage at the source of T 2 and rotate trimmers C 6 and C 7. Also here, a clear voltage maximum must be found. When due to a rotation of the core the oscillator stops operation, the voltage at the source of T 2 must drop by at least 0.2 V, provided that the injection frequency portion has been correctly aligned. C 5 remains fully rotated out.

5.11. Connect the frequency counter to the base of T 6 and pull both oscillators to nominal frequency (388.375; 389.25 MHz).

If the oscillator is oscillating too low, a small correction may be achieved by means of a little choke in parallel to the crystal (15 turns of 0.2 mm dia. enamelled copper wire wound on a 2 mm former).

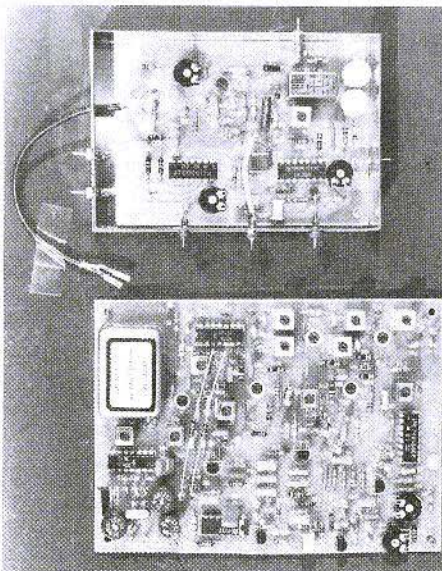
If the oscillator is oscillating too high, it is possible for the frequency accuracy to be improved with the aid of ceramic capacitors (4.7 to 10 pF), con-

nected in parallel to the crystal.

5.12. Provided that the frequency portion is o.k., the converter may be connected to a parabolic antenna ready for operation, and to a receiver; operating voltage at channel 1.

Now, the METEOSAT-signal should already be audible. If this is not the case, it will be necessary for C 3 to be tuned somewhat. The adjustment of C 3 is very critical, a rotation of some tenths of a millimeter will often be already sufficient. With the METEOSAT-signal being audible, C 1 to C 4 are adjusted several times one upon another to maximum insertion gain. An alignment of C 5 will practically not yield any additional improvement, since mostly it remains rotated out entirely. The 100 Ω potentiometer can be adjusted to minimum noise only at an NF measuring setup, otherwise it remains in its central position.

The final fine alignment is to be carried out with the cover placed into position on the conductor-lane side.



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Harald Hufenbecher, DL 6 NAD

A Digital Multiple Image Storage for Weather Satellite Images

Subsequent to the constructional descriptions of Matjaž Vidmar (YU3UMV) in VHF COMMUNICATIONS, Editions 4/82 and 1/83 on the digital storage and converter for weather satellite images, this article is to describe an extension of the storage which permits several METEOSAT images (max. 10) of the same section to be read in at temporal intervals and to be displayed later as a "film" on the screen. Thus, the observer gets the immediate impression of watching the cloud movement with a fast motion effect.

1. INTRODUCTION

Those of our readers who once had the chance to see one of the timelapse photographs of weather satellite images in an ESA TV-publication, certainly know that it is only this display which will lead to final conclusions. Practically at first view, one will obtain informations on direction and speed of meteorological conditions, where and how clouds, fogs, thunderstorms, or even whole low or high-pressure regions are building up or are decomposing, how they affect, support, or weaken each other.

For a realization, however, high demands are placed on the coincidence of the individual images transmitted. This can be ensured only by geo-

stationary satellites where the raw images are processed with the support of highly sophisticated software so that even a drifting of the satellite on its orbit can be compensated for. Already the author's first attempts proved that this problem has been taken care of in an excellent way by the ESA-staff.

Now we should deal with the remaining realization itself.

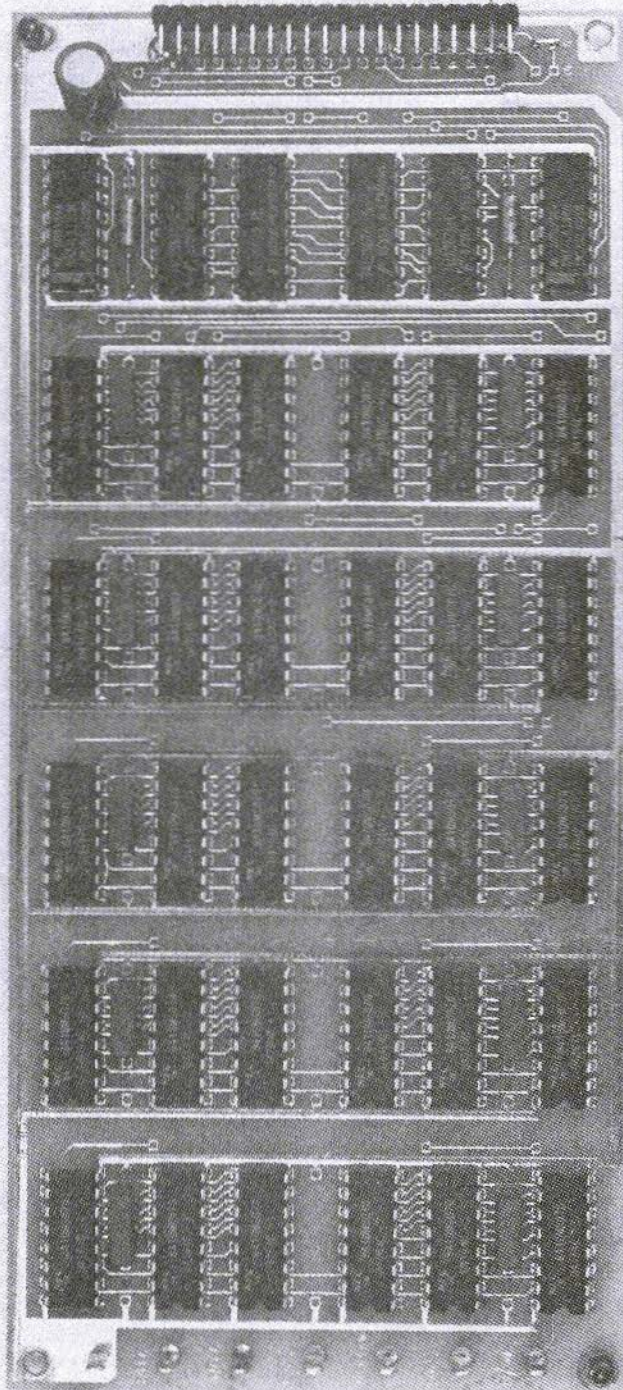
When considering the question of how to store a maximum of images with a minimum of storage effort, one will remember the procedure which in principle stores the variations from one image to the subsequent one. Both for analysis and synthesis of the storage contents this requires, however, a considerable hardware and software involvement which must provide moreover a video signal at the output, in other words must be very fast.

At the input one will have to expect – contrary to conventional TV-technology – an additional aggravating effect in form of a partly rather poor signal-to-noise ratio.

In view of the fact that the number of images to be stored would be not very high, with no colour information contained, that construction and circuitry should be reproducible, and the costs for integrated memory ICs are already at a reasonable level, a straight-forward circuit was developed. This circuit, it is true, represents a RAM-"grave" whose size could stimulate the envy of each "hobby-computer fan", whose control circuit, however, is relatively unexpensive.



Fig. 2:
Prototype of the
storage board
DL6NAD 002 (due
to delayed delivery,
it was not yet possible
for the tantalum
electrolytics to be
soldered in)





All those of our readers who are nevertheless afraid of the RAM-costs should know that the circuit – coded only by two wire bridges – can be furnished alternatively for three, five, eight, or ten images and be extended at a later date without any difficulties.

The circuit for three or five images is accommodated on two PC-boards. Both have the dimensions given by YU3UMV and are designated as electronic board (**Figure 1**) and storage board (**Figure 2**). For a possible later extension to eight or ten images, the storage board will be required twice. Before going into detail, however, a short description of the circuit itself should follow now.

In normal operation, released by a start tone, the corresponding memory sector is selected and the image read in, as is usual with YU3UMV modules. The stop tone automatically switches over to "film", and the images already written in are now read out in the time-lapse mode.

Empty or uninteresting images are neglected, in order not to disturb the film sequence in the case of a storage having not yet been entirely filled up. If the storage is full, i.e. the maximum number of images loaded, the oldest image will be overwritten by the next image. When reading out (film), one will start with the oldest image being present in the storage. This image remains visible for two clock times. It is followed, now in correct order, by the remaining contents up to the actual (last) image. This remains selected during five clock times, i.e. five times as long on the screen. Then the whole sequence starts anew. This means that at each extension stage the unit can virtually stay in continuous operation and one will have always access to the latest "survey".

As mentioned already at the beginning, the individual images must coincide. In order to ensure this also for sections or partial images, two four-pole DIL-switches or bridges have been provided whose settings (in binary code) can prematurely stop the image at a particular line number, when being read in.

In order to complete the main characteristics of the system, it should be mentioned that it is, of course, possible also for individual images, i.e.

images without any relationship among each other, as well as for images of orbiting satellites to be read in and displayed again independently.

2. ELECTRONIC BOARD DL6NAD 001

The whole circuit of this PC-board is shown in **Figure 3**.

The actual control function, i.e. the selection of the individual memory sector addressed, is taken over by an EPROM which operates in this circuit like a multifunction gate with 13 inputs and 8 outputs. By means of logic input signals, this component (I 109) receives via two coding switches or even only bridges, among others the information on the extension stage, on how many coherent images have been read in, and how they will be read out for the film. Here, the EPROM fulfills the function of a multiplexer. The subsequent 8-bit buffer storage is only to keep away the slow function of the C and N-MOS logics from the faster LS-ICs.

The second part of the control logic is a counter (I 110) fulfilling the function of the "scroll"-counter I 218 of YU3UMV 002. Here, it serves simultaneously as line counter for the premature stop at image sections. The counter reading, however, must be stored and reassigned to each image when being read out, in order to thus pass on the start address of each image to the address multiplexer on YU3UMV 002. This storage is performed by a 2Kx8Bit-RAM which is utilized only to a fractional part, but can be obtained at a low price and without any difficulties. A clock generator (I 101) determining the film speed completes the control logic.

2.1. Function Description

The author would like to start with this clock generator. It consists mainly of the well-known timer 555 (I 101) which can be employed here also in the CMOS-version (ICM 7555). Since a synchro-



nization with the video signals is not necessary (only the image content is changing) it is possible for the frequency to be continuously varied with the aid of R 101. In the dimensioning given, the clock time can be varied between approximately 50 ms and 850 ms. With the aid of C 101 it is possible to achieve an additional alteration according to one's own ideas. Two component positions (in parallel) are provided for this purpose on the PC-board.

Due to the relatively low-impedance discharge resistance of 150 Ω , there will result at the output (I 101/3) only short low-pulses with a width of approximately 230 μ s; its falling slope clocks the counter I 107 a. This 4-bit binary counter determines the image sequence during the film. The rising slope represents the strobe pulse for the 8-bit buffer storage (I 108).

When being switched on, I 115 a will generate an approximately 8 ms long reset pulse by which the buffer storage is reset, and thus also the RS-FF realized together with the EPROM, as well as counter I 107 b, which serves as image counter.

Having described now the auxiliary circuits, we may go more into detail.

2.1.1. Film

The film run is released by a low-signal (L) at one of the inputs of gate I 102 d. This can be applied either by the closed switch "Film" (S 101 a), or by a clock or a timer which may be connected here, or even activated by the start-stop signal from YU3UMV 001.

From these linked signals there will result a $\overline{\text{Write}}$, and via the NAND-gate subsequently coupled as inverter, a Write signal. Via I 102 b and I 104 d this Write (now L) releases the binary counter which – as mentioned already – counts the clock pulses. In parallel, also the EPROM receives the information Write (L) and thus recognizes that the operating mode "Film" is concerned. The corresponding counter reading is coded via the internal program that generates the film sequence, and fed to the image address lines to the second PC-board.

The count limit is determined by the number of read-in images available, as mentioned already,

in the second binary counter (I 107 b). If this limit is reached, the EPROM will put out an L-signal on Q₆ (pin 18), resetting counter I 107 a via the NAND-gate. Approximately 10 μ s after the resetting, the differentiation with the aid of the 1 nF-capacitor will produce a rising slope with which the new state at the EPROM will be immediately written into the buffer storage.

With the aid of $\overline{\text{Write}}$ (H), I 110 will be disconnected by I 112 and I 113, while I 114 will be switched with the aid of Write to the eight lines leading to PC-board YU3UMV 002.

All further circuit parts of the control logic are virtually of no importance in this operating mode.

2.1.2. Loading

For this purpose, the switch "Film" must be opened at I 102 d, i.e. must stand on "Write In", and a connected timer must go to High (H). With the start of an image, $\overline{\text{Write}}$ becomes L and Write becomes H. Via I 105 b this causes a release of the line clock pulses from Pt 124 to Pt 205, and a reset of the scroll counter, differentiated by an 1 nF capacitor and inverted with the Schmitt trigger I 104 c. This pulse (approx. 10 μ s) now switches forward also the second image counter by one position. As can be seen, however, this pulse remains neglected, if switch S 102/3 a is closed, if this is the case, the **last image loaded is overwritten by this image just started.**

In this way it is possible also for images not pertinent to the film to be recorded without destroying it by a "wrong image". The limit of this counter determines the extension stage which is disclosed to the EPROM with the aid of bridges "A" and "B":

Extension stage	Bridge at
3 images	none
5 images	A
8 images	B
10 images	A and B



As soon as the limit is reached, a reset signal will be output, just as with the aforementioned counter, this time, however, at Q_7 (pin 19).

At the same time, an H will appear at Q_5 (pin 17), which is taken over by the buffer storage and fed back to an address input. This circuit, which may seem a little bit "obscure" at first sight, represents the mentioned RS-FF and serves for storing, no matter whether all installed image storages contain a valid image, i.e. must be read out, or not.

When loading an image into the storage, I 110 counts the scroll clocks in order to effect a scroll of the image, as we have seen already with I 218 on YU3UMV 002, and moreover to cause a premature stop since the number of scroll clocks is identical with the line number. Due to the little trick of applying the pull-up resistors of I 111 to Q_9 , the minimum line number is 256 and may be arbitrarily set in the binary code in steps of 16 lines, each. Since a displayed image has 256 lines, a lower adjustment would not be useful.

A setting for an automatic stop can be activated by closing one of the two switches (S 102/5 for S_1 and S 102/6 for S_2). If both switches are open, the read-in process will be terminated, as usual, with the stop tone. Besides, the latter must be waited for also in the case of an automatic stop, since it is this stop tone that causes the unit to automatically change over to the operating mode "Film".

2.1.3. Single Frames

If switch S 102/2 is closed for this purpose, this will prevent counter I 107 b to be affected by the remaining electronics via gate I 102 b. Now, each counter reading will be directly connected with the image address, no matter what is being present at the other addresses of the EPROM.

By means of the clock counter it is thus possible for **all installed image storages** to be selected one after the other.

When reaching the desired image, S 102/1 is closed, the clock generator stops, and the selected memory sector can be utilized quite normally, without interfering with the remaining sectors, yet with the advantage that with the aid of S 102/2 it

will be possible for this image to be reselected at a later time and displayed again.

2.1.4. Controls

Now the author would like to give a short survey on all control elements and their functions:

- R 101: Frame speed (potentiometer 500 k Ω)
- S 101: Film/write-in (1 opening, 1 closing s.)
- S 102/1: Single-frame selection, stop 1)
- S 102/2: Single-frame selection, search 1)
- S 102/3: Film construction, write over last image
- S 102/4: Film construction, stop with stop-tone
- S 102/5: Film construction, stop via switch assembly S 1
- S 102/6: Film construction, stop via switch assembly S 2

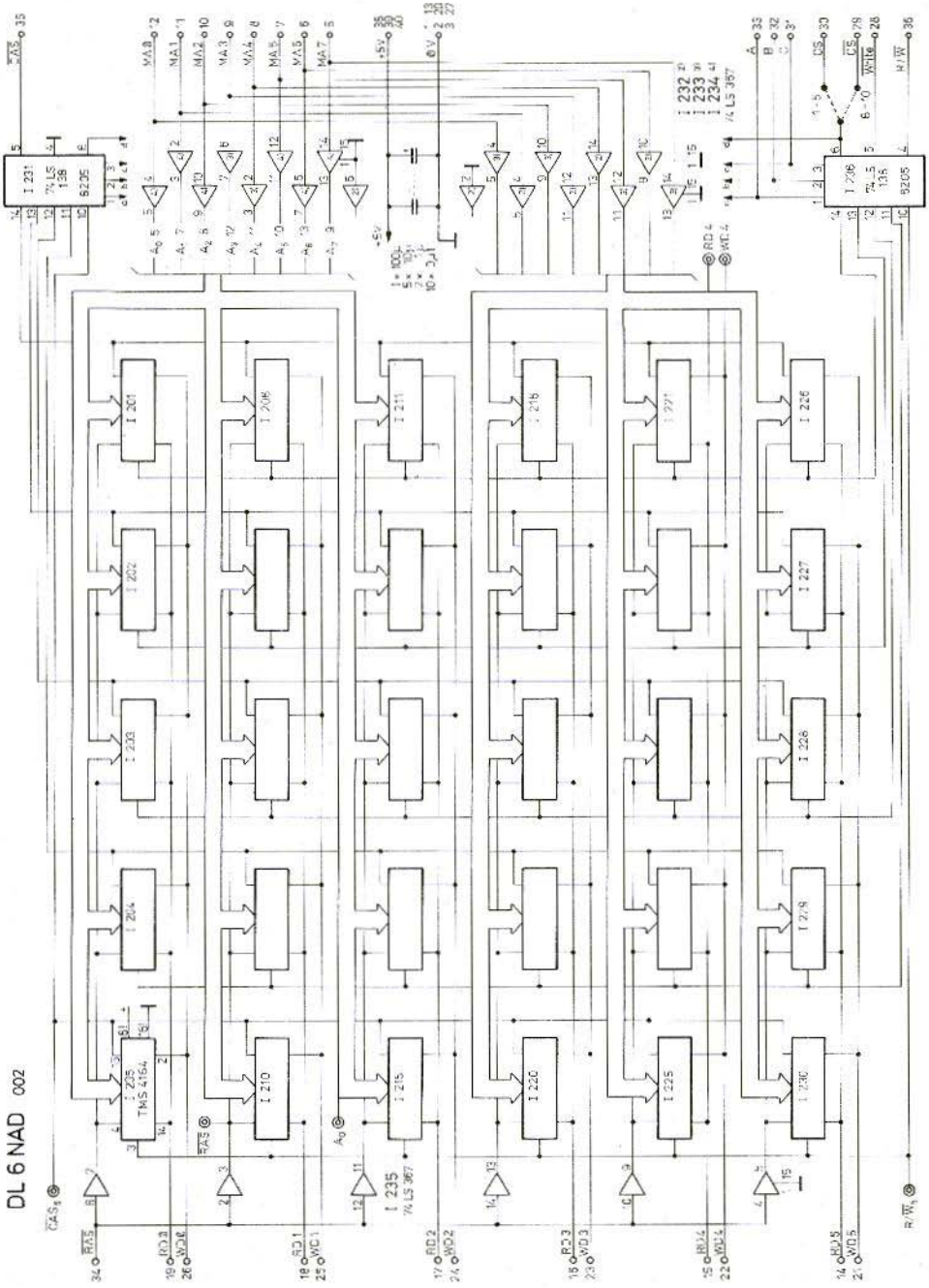
1) Resets the film image counter for a new film construction.

It is possible for **S 101** to be mechanically coupled with potentiometer R 101 (e.g. pull switch); it replaces the stop switch used so far.

S 102 can consist of a useful combination of individual toggle switches, or be realized with a two-level/six-step rotary switch, – this will always depend on the individual ideas, or the facilities on the front panel.

3. STORAGE BOARD DL6NAD 002

This PC-board whose circuitry can be seen in **Figure 4**, is provided with the component positions for thirty 64K-DRAMs, i.e. the memories for five images of 6 Bit, each, furthermore the drivers for address and \overline{RAS} lines, as well as the 3-bit binary decoders employed as demultiplexers, for distributing the \overline{CAS} and R/\overline{W} signals. For the third and fourth extension stage, i.e. eight and ten images, two of these PC-boards will be required. It will then only be necessary to determine with the aid of a wire bridge on the corresponding PC-board, whether the memories for images 1 to 5, or 6 to 10 are concerned.



DL 6 NAD 002

Fig. 4: Storage circuit DL6NAD 002 for max. 5 WEFAX images



3.1. Function Description

In this assembly, the memories work in the same manner as those used in the circuit of YU3UMV. Therefore the author may take this as common knowledge. Neglecting now in our further considerations the drivers (74 LS 367), one could state that all equal-valency addresses of the RAMs are in parallel, that all data inputs or outputs of equal valency are also in parallel, and that all $\overline{\text{RAS}}$ -connections are interconnected.

The selection, i.e. which memory sector is active, is determined by the $\overline{\text{CAS}}$ -pulses. Only when this $\overline{\text{CAS}}$ -signal goes to low-level, the output of the storage will be switched onto the data line. This means that this signal will not only release a $\overline{\text{CAS}}$ but also a so-called "Output-Enable", i.e. an activation of the output.

The selection of the correct $\overline{\text{CAS}}$ -line is carried out by the fast 3-bit binary decoder 74 LS 138 or SAB 8205. In addition to the (image) address inputs, it possesses three release inputs. The $\overline{\text{CAS}}$ -signal derived from PC-board YU3UMV 002 is fed in via one of these inputs. Depending on the image address being applied, the $\overline{\text{CAS}}$ -clock appears at one of the five outputs.

In the same manner, a second decoder handles the $\overline{\text{RW}}$. In addition, however, this component is either blocked or released by means of the Write information of the control logic.

4. CONSTRUCTION

The control logic is accommodated on PC-board DL6NAD 001 (Figure 5) and the memory module on PC-board DL6NAD 002 (Figure 6). In their dimensions and fastening points they correspond, that is true, to the PC-boards of YU3UMV, they are, however, not only double-coated but also through-contacted. In order to avoid greater trouble, please, pay utmost caution and care during the component locating and soldering process !!

4.1. Components

There were no "exotic" components used, nevertheless the author would like to give the following hints:

It is possible for the 8Kx8-Bit EPROM (I 109) whose speed does not play a demanding role (450 ns are sufficient), to be programmed on an appropriate device with the bit pattern (a list may be obtained from the editors) by our readers themselves, or to be supplied ready-made.

The resistors in the circuit diagram which show numbers within the symbol, are part of a resistance network. The construction can be single or dual in-line. Yet a conventional installation of individual resistors is also possible.

The connectors are double-row pin connector strips with a spacing of 2.54 mm, taken from computer technology.

The 100 nF bypass capacitors are ceramic multi-layer MKH, MKM, or MKS types. The values of 1 μF , 2.2 μF , and 10 μF are tantalum electrolytics which must have an axial design, especially on the storage board, in order to avoid long leads. For the 64 k memory-ICs the same conditions are valid, as were described in VHF COMMUNICATIONS, Edition 1/83. The author would like to emphasize once again that here only and exclusively those memories may be used which permit page mode operation !!

It is certainly superfluous to say that with all CMOS ICs only the B-series should be used and that one should never use cheap sockets, but try and better do without them at all. Only for I 109, i.e. the EPROM, a 28-pole socket is recommended since here, due to a different functional sequence or operation, something might change.

4.2. Modifications on YU3UMV 001 and 002

On the electronic board YU3UMV 001 an additional connection point needs to be provided only in the area of the tone decoders and the synchronization logic. It is connected with pin 11 of I 115 (CD 4011) and is designated Pt 131.

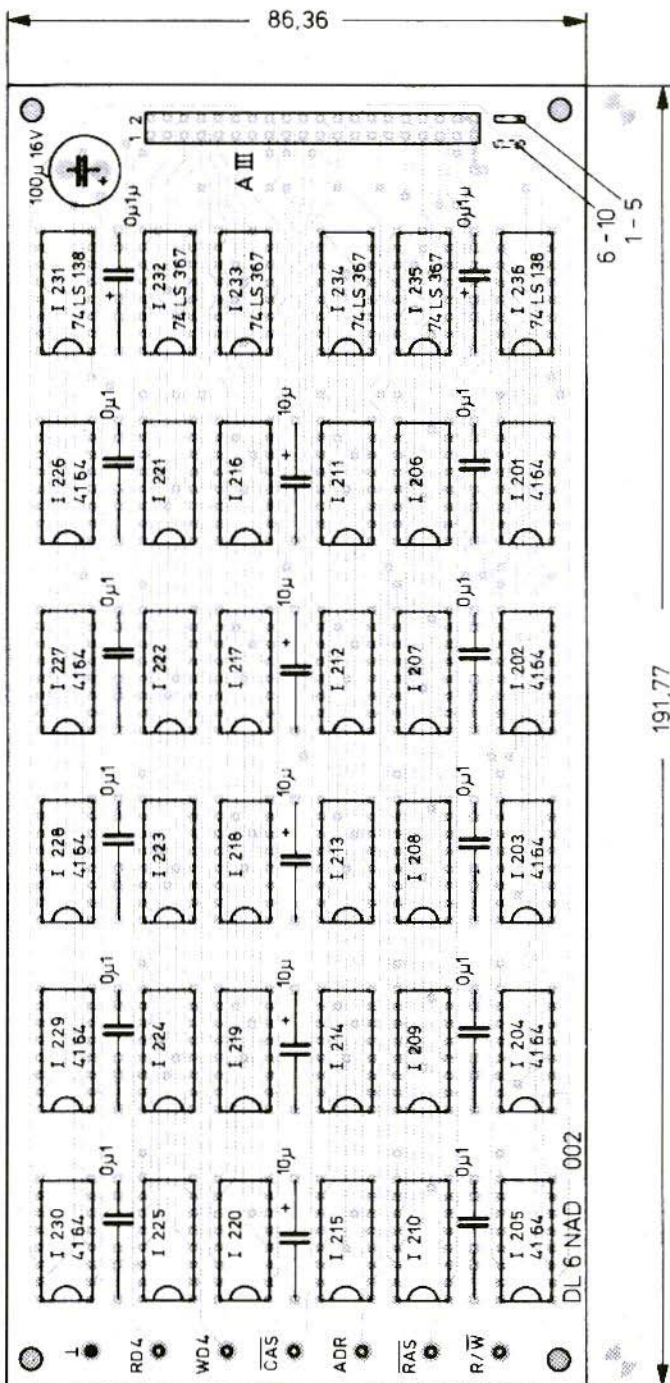


Fig. 6:
Component location
plan of the storage
board DL6NAD 002

It is in the same part of the circuit, that the 4.7 k Ω resistor between pins 5 and 10 of I 116 must be bridged with a diode (e.g. 1N 4148). The cathode (line) shall lie on 5, the anode on 10.

In the case of a new construction of PC-board YU3UMV 001, type CD 4093B should be used each for I 115 and I 116, which, due to its Schmitt trigger characteristics, will create after all those R-C links defined slopes again.

On the second PC-board YU3UMV 002 work will be somewhat more extensive, yet feasible, indeed (courage!). Here, the most difficult task should be considered in the removal of two ICs: I 218 (CD 4040) and I 212 (74 LS 123) must be carefully removed from the board without causing any damage.

Unfortunately, it is necessary for all six memory ICs, namely I 225 to I 230, to be removed!

Now the resistor (1k) between I 210/12 and + 5 V is exchanged against a value 2k Ω .

For I 212 a somewhat faster type, a 74123 or a 74LS221, will be employed. Previously, however, the connections to pin 11 of this component on the PC-board (solder and component side) are to be interrupted and interconnected again among each other. Pin 11 (free) should be applied with a resistor of 1 k to + 5 V (pin 16). Furthermore, the connection from pin 10 to pin 13 of the same IC on the PC-board is separated and pin 10 newly connected with pin 4. If now a small 10 pF capacitor is soldered between pins 14 and 15, the worst will be over.

What remains now to be done, is to separate at I 217 (74LS 04) on the solder side the connections from pin 4 to pin 6, from pin 2 to pin 3, and from pin 3 to pin 5. A resistor of 330 Ω will now be soldered between pins 2 and 5, and a capacitor of 120 to 150 pF will be soldered also at pin 5, but against ground (pin 7).

This concludes the constructional conversion, yet the whole assembly should remain within reaching distance for the subsequent wiring process.

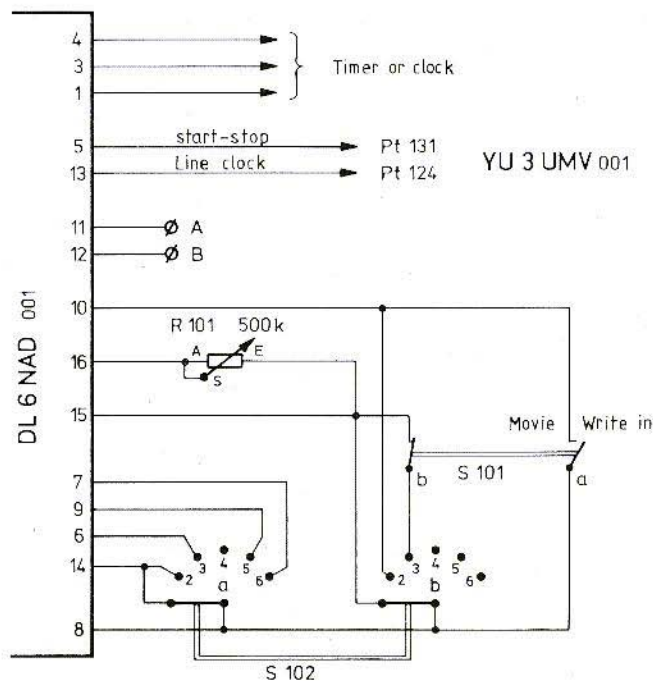


Fig. 7:
Wiring DL6NAD 001
- YU3UMV 001 -
Controls - clock



4.3. Wiring

The wiring of the PC-boards among each other and to the control elements is very simple and consists mainly of three stages.

I. To the Front Panel (A I)

With the aid of the 16-pole connector A I all connections are made to the assembly YU3UMV 001, to the control elements, and also to the clock or to a timer. Details of the wiring are shown in **Figure 7**.

II. To YU3UMV 002 (A II)

Connection A II comprises a 14-pole flatband cable with two crimp connectors in DIL-spacing. One of these connectors is **soldered in** at the position where counter I 218 was located, in a way that the holes for pin 1 and pin 16 of I 218 remain free. Line 14 takes over the task of Pt 205 of this PC-board, however, must be tied to this connection with the aid of a wire, preferably on the solder side.

III. Bus Line (A III)

This line connects PC-boards YU3UMV 002, DL6NAD 001, and the one or the two storage board(s) DL6NAD 002.

The connection itself comprises **one** 40-pole flatband cable with a spacing of 1.27 mm, being provided also with 40-pole jack connectors of the crimp type. The correct spacing, i.e. the position of the connectors on this line is determined by the constructional design.

If the mentioned PC-boards are, for instance, mounted one upon another with the aid of spacer bolts, it should be most easy for this wiring to be carried out. Each PC-board will then be provided with an appropriate connector through which the short cable is only looped through. The sequence of the PC-boards is of no importance here and can still be exchanged at a later time for measuring purposes. Since, however, the previously published PC-board is unfortunately not prepared for this system, it becomes necessary now for the cable to be spliced at one end, and for the leads to be individually soldered to the corresponding points on the PC-board.

It will be useful to proceed here according to the following list which shows also the pin and cable locations on the whole connector.

No.	Designation	Aim at YU3UMV 002
1	ground	ground
2	ground	ground
3	ground	ground
4	free	—
5	MA 7	I 225/9
6	MA 6	I 225/13
7	MA 5	I 225/10
8	MA 4	I 225/11
9	MA 3	I 225/12
10	MA 2	I 225/6
11	MA 1	I 225/7
12	MA Ø	I 225/5
13	ground	ground
14	RD 5	I 231/3
15	RD 4	I 231/4
16	RD 3	I 231/14
17	RD 2	I 231/13
18	RD 1	I 231/11
19	RD Ø	I 231/6
20	ground	ground
21	WD 5	I 230/2
22	WD 4	I 229/2
23	WD 3	I 228/2
24	WD 2	I 227/2
25	WD 1	I 226/2
26	WD Ø	I 225/2
27	ground	ground
28	Write	—
29	CS	—
30	CS	—
31	C	—
32	B	—
33	A	—
34	RAS	I 210/12
35	CAS	I 217/4 or 6
36	R/W	I 217/10 or 12
37	free	—
38	+ 5 V	
39	+ 5 V	see following
40	+ 5 V	text

No. 1 is the conductor or pin identified on the flatband cable by colour, and on the connector mostly by an arrow or triangle.

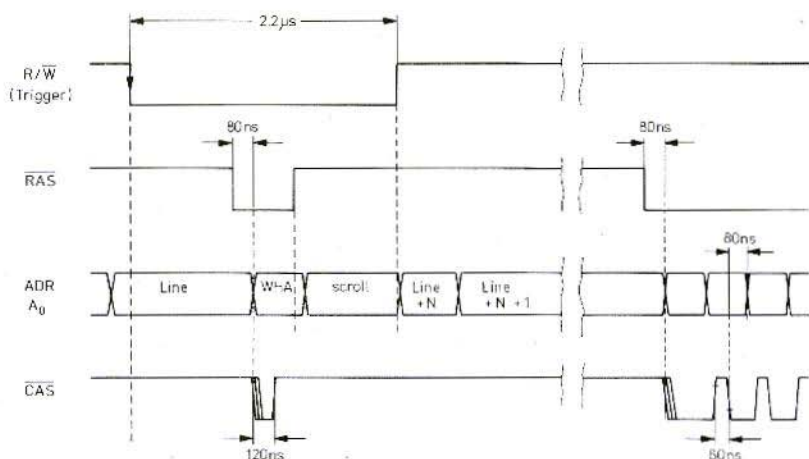


Fig. 8: Pulse diagram of circuit DL6NAD 002

A replacement for PC-board YU3UMV 002, being compatible with this array without any modifications, is being prepared and will be published at a later date.

5. COMMISSIONING

The power requirement of the additional PC-boards is typically 250 mA, without the memories.

Since the memory ICs of 64 k, each, are indicated with approx. 40 mA (max.), the author had expected an additional current drain of approx. 1.2 A (at 5 V and with five frames). He was surprised at the result of his measurements which showed that the measured value per frame, i.e. six memories, increased only by approximately 10 to 20 mA. Since it is not possible to derive herefrom a definite conclusion on the actual power consumption that has to be expected, the author desisted so far from connecting the 5 V-supply with the + 5 V of the YU3UMV PC-boards. Whether this would be possible without overloading the regulator, also depends to a considerable extent on the heat sink and must be clarified from case to case.

If one has ensured once more, at least visually, that all ICs are in their correct position (all identifications in one direction), that no electrolytic is incorrectly polarized, that all plug connectors (not displaced) are connected, and that the bridges on

the PC-board(s) are correctly placed, it may be switched on, under the prerequisite, of course, that at least PC-board YU3UMV 001 has been aligned as far as possible.

A number of measuring points have been provided on the PC-board for checking the signals necessary for the storages. If required, they can be connected with an oscilloscope.

When loading into the fifth or tenth image store, the diagram shown in **Figure 8** must result.

It is absolutely necessary to consider that the falling slope of the CAS may occur only **after**, and at best **with** the change of the address ADR. If this is not the case, irregular, vertical stripes will appear during the inputting process. It might become necessary, for delay purposes to somewhat enlarge the mentioned 120 pF capacitor.

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Harald Braubach, DL 1 GBH

A Power Meter for the Frequency Range from 2 to 200 MHz

There are many ways to construct a power meter. The most simple way is to use a diode with subsequent DC-amplifier. This has the disadvantage that a high temperature drift is present, especially at low RF-levels, which must be corrected for with the aid of extensive compensating circuits. In addition to this, the calibration of the scale is not the same in all measuring ranges.

Another method is to provide gain in front of the diode and to keep the power level at the diode constant in all measuring ranges. This has the advantage that hardly any temperature drift of the DC-voltage is noticeable, since it is far less than the rectified voltage of the diode.

The scale calibration will be the same for all ranges, since the diode is always operated in the same power range. This article is to describe such a meter.

1. PRACTICAL CONSTRUCTION

A three-stage wideband amplifier with a gain of 10 dB per stage is used for amplifying the RF-signal. The circuit of this preamplifier is given in Figure 1. Since it is very difficult to connect the

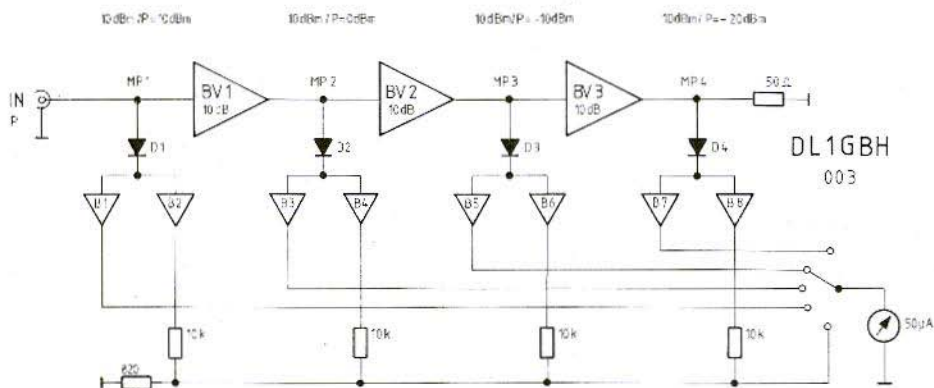


Fig. 1: Principle of a power meter using wideband amplifiers and separate rectifier diodes for each 10 dB range

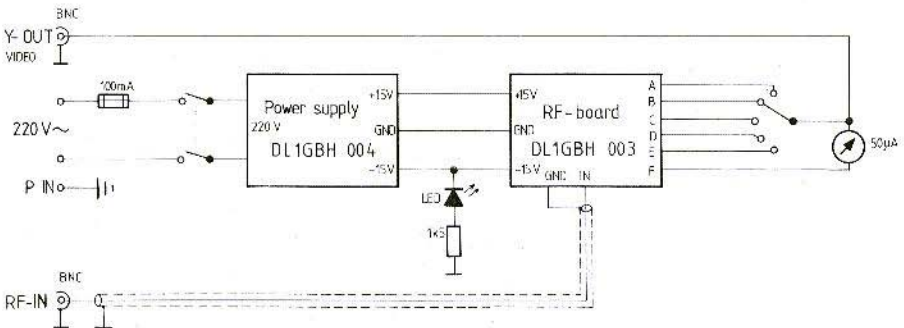


Fig. 2: The circuit of the power meter is divided over two boards and provides an oscilloscope output for swept-frequency measurements

RF-side of the diode to the various test points MP 1 to MP 4, each test point has been provided with its own diode, and their output DC-voltages are fed via amplifiers (B1, B3, B5, B7) to the range switch.

The first diode connected to MP 1 is used for input power levels from 0 dBm to +10 dBm. The diode connected to MP 2 is for the range from -10 dBm

to 0 dBm, the diode at MP 3 from -20 dBm to -10 dBm, and finally the diode at MP 4 for the range -30 dBm to -20 dBm.

This means that a level of between 0 dBm and +10 dBm is present in each measuring range. This allows virtually the same scale to be used for all measuring ranges. Of course, this is only valid when all amplifiers are operating within their line-

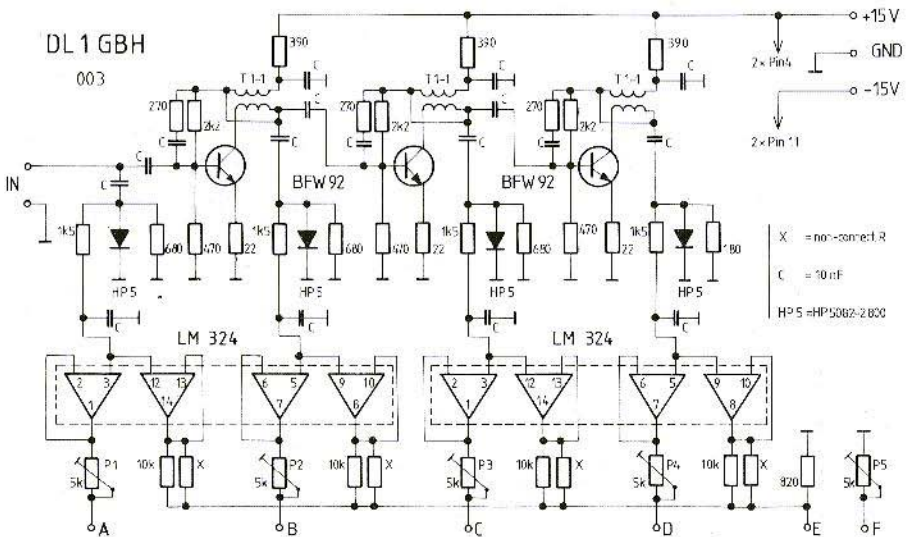


Fig. 3: The three, wideband amplifiers are constructed using inexpensive UHF-transistors and available wideband transformers

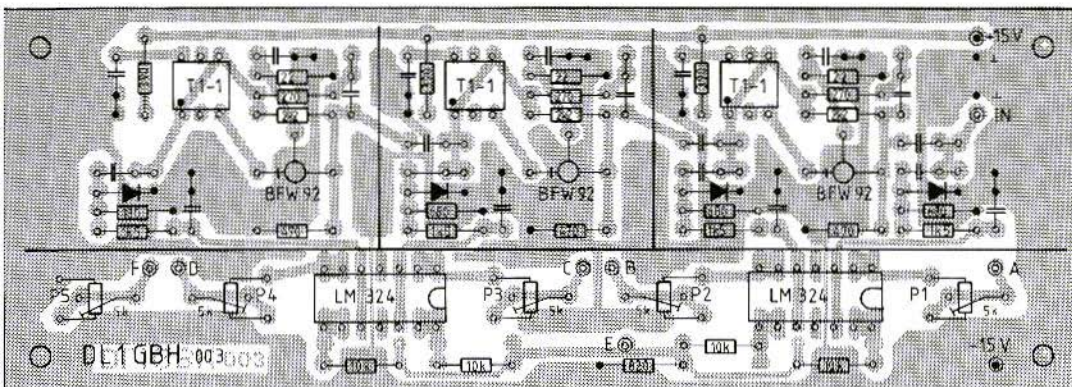


Fig. 4: Component location plan of the power meter board. The upper side of the board is in the form of a continuous ground surface onto which the ± 15 V connections are made, and from which the copper surface must be removed with the aid of a drill

ar range. The wideband amplifiers used have a maximum output power of +15 dBm, and this ensures that this demand is met.

A further possibility results when using this principle, if the output voltages are converted into proportional currents, and then added. In this manner, it is possible to obtain a quasi-logarithmic reading over a range from -20 to $+10$ dBm. This can be very advantageous, for instance, when aligning filters. One simple method of converting voltages into proportional currents is to feed the voltages via high-impedance series resistors (10 k Ω) to an adding point, where they are added across a low-impedance resistor (820 Ω). The amplifiers B2, B4, B6, and B8 are used for decou-

pling between the stages.

2. SWEPT-FREQUENCY OPERATION

Since the upper limit frequency of the rectifier circuit amounts to approximately 5 to 10 kHz, it is possible for the power meter to also be used for detecting the envelope of RF-signals. A further advantage of the fast rectifier circuit is that it can also be used for swept-frequency measurements. This is favorable, for instance, for the alignment of power amplifiers (as described in VHF COMMUNICATIONS 3/1983).

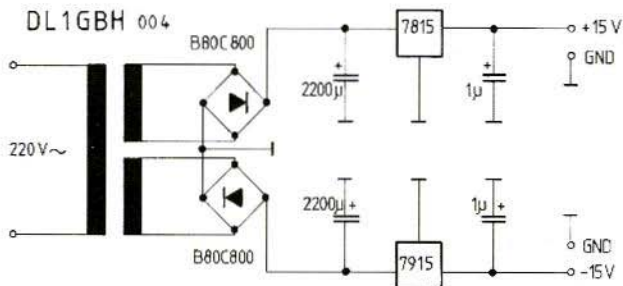


Fig. 5: The ± 15 V power supply with integrated voltage stabilizers



Filters can be aligned more exactly when a logarithmic indication is used in swept-frequency measurements. Since the meter is too slow for such applications, the rectified voltage from the diodes is available at a BNC-connector on the front panel (**Figure 2**). During swept-frequency measurements, it is possible to connect the Y-deflection of the oscilloscope to this connector.

3. THE RF-BOARD

Printed circuit board DL1GBH 003 was designed for accommodating the circuits of the preamplifier, diodes, and buffer amplifier shown in **Figure 3**. The dropper resistors for aligning the meter are also accommodated on this board. An individual trimmer potentiometer is provided for each range, as well as a potentiometer for aligning the logarithmic range. **Figure 4** shows the component locations on this double-coated PC-board, whose dimensions are 146 mm x 51 mm. The components T1-1 are wideband transformers from Mini Circuits, type MCL T1-1.

4. THE POWER SUPPLY BOARD

The simple ± 15 V power supply shown in **Figure 5** can be accommodated on the single-coated PC-board DL1GBH 004. The component locations are shown in **Figure 6**.

5. CONSTRUCTION

The PC-boards should be provided with the components according to the component location plans and be mounted with the aid of 10 mm spacers to the base plate of a suitable cabinet. The meter is installed into the front panel, as are power switch, LED, range switch, and the BNC-connectors. A power line connector or feed-through are provided on the rear panel together with the fuse holder.

The power meter can then be wired as shown in **Figure 2**. A 50 Ω coaxial cable is only necessary for the RF-input. **Figure 7** shows the completed boards.

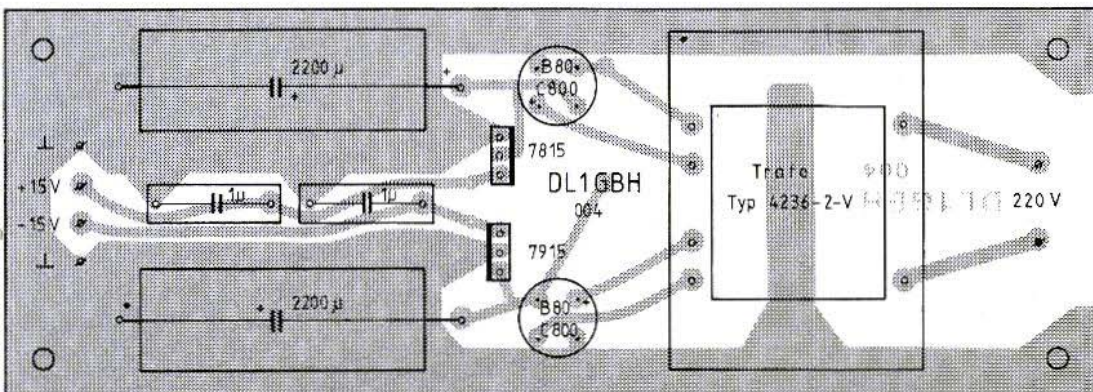


Fig. 6: Component locations on the power supply board whose dimensions are 146 mm x 51 mm

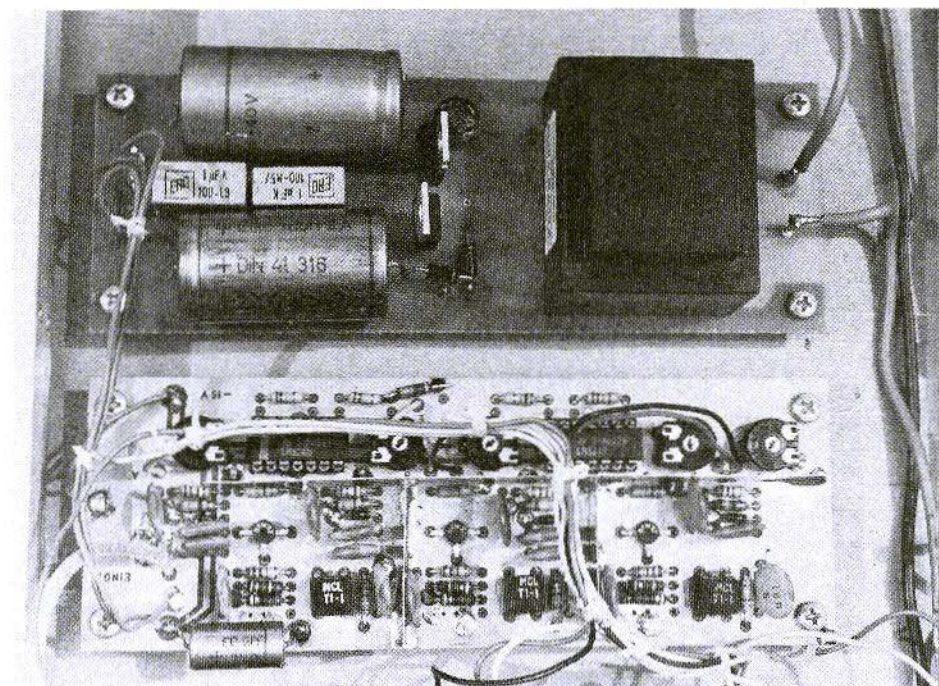


Fig. 7: PC-board DL 1 GBH 003 and 004

6. ALIGNMENT

The alignment is firstly carried out in range E. This is made by feeding a signal of +10 dBm (frequen-

cy approx. 145 MHz) and aligning P5 for full scale: this is followed by aligning range A with P1 at the same level.

Connect a level of 0 dBm, and align range B with the aid of P2; this is followed by the -10 dBm-range C (P4), and the -20 dBm-range D (P4).

Measuring frequency	9 MHz	18 MHz	36 MHz	72 MHz	144 MHz	
Scale	P_{in}/dBm	$I/\mu A$	$I/\mu A$	$I/\mu A$	$I/\mu A$	
0 dB	+10	50	50	49	48	50
-1 dB	+9	43	43	42	40	44
-2 dB	+8	35	34	34	32	36
-3 dB	+7	28	27	27	26	30
-4 dB	+6	22	21	21	19	24
-5 dB	+5	17	16	16	15	19
-6 dB	+4	12	12	12	11	15
-7 dB	+3	9	9	9	8	11
-8 dB	+2	7	7	7	6	8
-9 dB	+1	5	5	4	4	6

Table 1:
Scale calibration of the author's prototype, measured in range A with signal generator HP 8640 A



The scale is calibrated either with a signal generator, or according to **Table 1**. The error caused by the spread of the diodes is relatively low.

As can be seen in the table, the reading is very constant over the whole frequency range. This means that the calibration can be made at virtually any frequency between 9 MHz and 144 MHz.

The logarithmic scale is calibrated in 10 dB-steps, as shown in **Table 2**.

Scale	P_{in}/dBm	$I/\mu\text{A}$
+ 10	+ 10	50
0	0	34
- 12	- 10	16
- 20	- 20	4

Table 2

The scale of the meter is removed carefully from the meter itself for marking. This can be made by painting over the numbers (Tippex) and providing the new scale with the aid of rub-on digits after drying. The scale of the author's prototype can be seen in **Figure 8**.

7. MEASURED VALUES

An input VSWR of less than 1.2 was measured on the author's prototype between 2 MHz and approximately 160 MHz. The voltage standing wave ratio only started to increase in excess of 160 MHz up to a value of approximately 1.5 at 200 MHz. For those applications where better matching is required, it is possible to provide an attenuator in the input circuit, however, with some reduction of sensitivity.

As you probably know, an attenuator will reduce the input signal by the given value, however, the reflected signal will be reduced by twice this value. In order to obtain a VSWR of better than 1.2 over the whole frequency range, it would be necessary to provide an attenuator of 3 dB. This, of course, assumes that the attenuator itself has a VSWR of far less than 1.2 when correctly terminated.

Figures 9 and 10 show the frequency dependence of the reading in the various power ranges. Figure 9 shows the frequency response of the logarithmic range at four different input levels. The in-

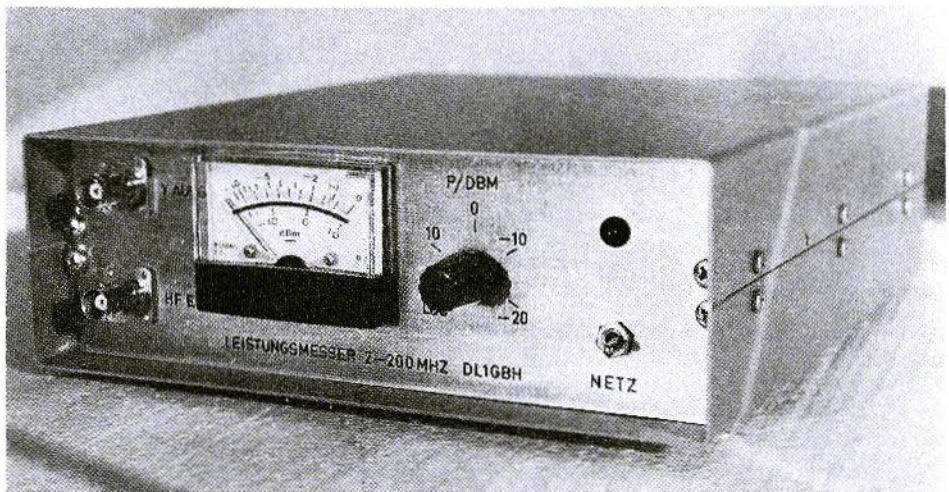


Fig. 8: Photograph of the author's prototype

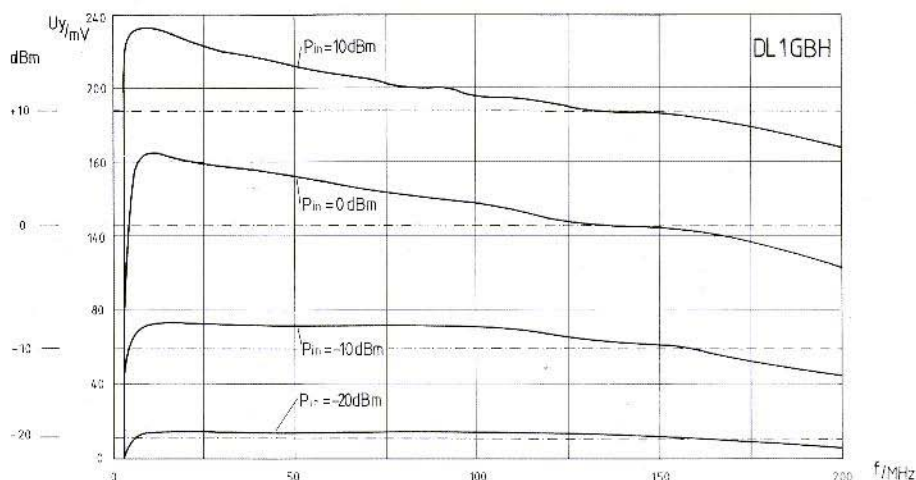


Fig. 9: Frequency response of the output voltage in the logarithmic range at four different input levels

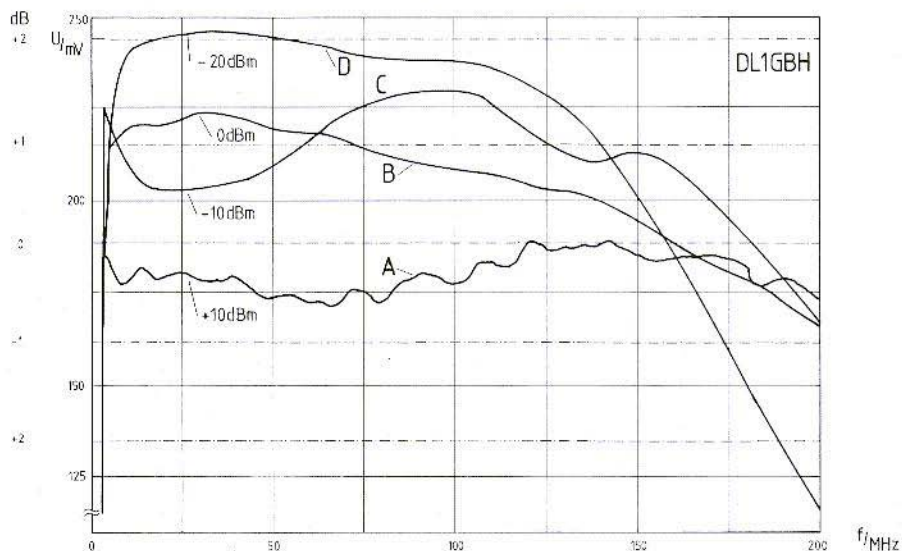


Fig. 10: Frequency response of the linear ranges

crease at lower frequencies and higher levels is caused by the different compression points of the wideband amplifiers at different frequencies. Figure 10 shows the frequency response of the linear range.

The +10 dBm-range is the one with the lowest frequency dependence. It is this range that does not have any amplifier with an intrinsic frequency

response. This range provides an accuracy of approximately 1 dB over the whole frequency range.

In the case of the subsequent ranges, the frequency response of the amplifier stages will be increasingly noticeable, however, the maximum error is still only 2 dB. The author's power meter was aligned so that it operated correctly at 145 MHz.



Erich Stadler, DG 7 GK
Elektronikschule Tett nang

Impedance Transformation using a $\lambda/4$ Line

Design Criteria using a Smith Diagram or BASIC Program

A line or a waveguide will “transform“ a real or reactive impedance or a combination of the two. According to the impedance of the transformation line, it is possible to transform a low real impedance to a high impedance, or a high impedance to a low impedance. An inductive reactive component will be converted to a capacitive, or a capacitive to an inductive component.

The latter is especially of interest in waveguide technology; in this case, screws can be inserted into the waveguide at a certain distance from a point of discontinuity, for instance at a spacing of $\lambda/4$. The waveguide transforms the capacitive effect of the screw (see **Figure 1**) to an inductive component at the position of discontinuity.

The real impedance transformation using a $\lambda/4$ line is well known: The required impedance is obtained from the simple equation:

$$Z = \sqrt{Z_{out} \times Z_{in}}$$

where Z_{out} is the terminating, and Z_{in} is the required input impedance of the $\lambda/4$ line.

Example: Four parallel-connected 50Ω resistors are to be matched to the output of a transmitter having an output impedance of 50Ω (for instance four antennas at 144 MHz). Required is the Z of the transformation line.

Solution: The four consumers form a terminating resistance of $Z_{out} = 12.5 \Omega$. The Z_{in} of the $\lambda/4$ transformer should coincide to the output impedance

Z_{out} of the transmitter: 50Ω . The following will result:

$$Z = \sqrt{12.5 \times 50 \Omega} = 25 \Omega$$

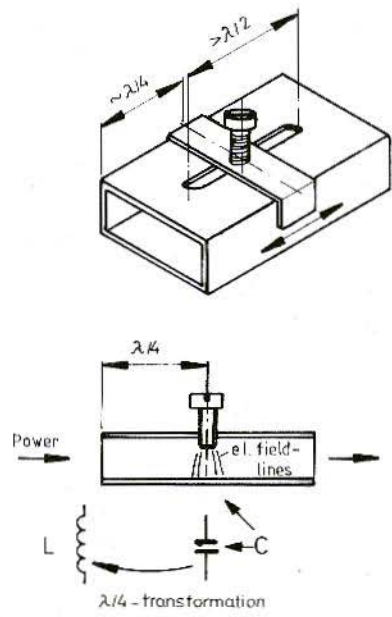


Fig. 1: Operation of the sliding screw tuner

This $\lambda/4$ -transformer can be obtained by connecting two 50Ω cables in parallel. Assuming a velocity factor of 0.66, this will result in the following for the 144 MHz band: $0.5 \text{ m} \times 0.66 = 0.33 \text{ m}$.

If Z and Z_{out} are given, Z_{in} will result by conversion of the equation:

$$Z_{in} = Z^2/Z_{out}$$

An input reactive impedance can be calculated in a similar manner if the $\lambda/4$ transformer is terminated with a pure, reactive impedance X_{out} :

$$X_{in} = Z^2/X_{out}$$

The equation does not give any information regarding the sign (plus in the case of an inductive, and minus in the case of a capacitive reactive component). One will have to remember that a capacitive reactive component X_{out} will result in an inductive reactive component X_{in} , and vice versa (Figure 1). The sign would be available only when doing a complex calculation !

Example: A 12 cm long line ($\lambda/4$ at 433 MHz assuming a velocity factor of approx. 0.66) of $Z = 50 \Omega$ is terminated with $C = 4.7 \text{ pF}$. Which L will result at 433 MHz ? (with 4.7 pF , X_{out} is approx. -78Ω).

Solution: $X_{in} = (50^2/78) \Omega$. The sign " - " of the capacitive reactive component of X_{out} is not used. X_{in} is inductive and corresponds to an $L = 11.7 \text{ nH}$ at 433 MHz.

The given equations are no longer suitable when the line is terminated with a series circuit of real and reactive impedances. A clear method can be found when using a Smith diagram, if one is used to working with it: The terminating impedance comprising a real and reactive impedance is standardized to the impedance Z of the $\lambda/4$ -line to be used and inserted (W_{out}). The resulting input impedance is found in the Smith diagram diametrically opposite (W_{in}).

Example: The input connector of a power amplifier is connected via a $\lambda/4$ stripline with an impedance of 20Ω to the relatively low input impedance of the power transistor of, for instance, 5Ω in series with an (inductive) reactive impedance of $+4 \Omega$. The two impedances form thus Z_{out} and X_{out} of the stripline and are transformed to a certain impedance at the input connector. The transformed values Z_{in} and X_{in} are to be calculated !

Solution: Standardize Z_{out} and Z_{in} (in other words divide by the Z of the line):

$$Z_{out}' = 5 \Omega / 20 \Omega = 0.25; X_{out}' = +4 \Omega / 20 \Omega = +0.2$$

Both values are now inserted into the circular coordinates of the Smith diagram (Figure 2); (a positive X_{out}' means "inductive" which means the upper part of the diagram).

The result is point W_{out}' . Diametrically one will obtain W_{in}' . Attention should be paid that the straight line really passes through the center of the horizontal line. This means that W_{in}' will have the same spacing from the center point "1" as W_{out}' . One then reads off the coordinates of W_{in} as:

$$Z_{in}' = 2.5 \text{ and } X_{in}' = -2$$

The negative sign represents a capacitive reactive component of W_{in}' . The values are "destandardized" by multiplication with the standard impedance, and one will obtain the input impedance as:

$$Z_{in} = 2.5 \times 20 \Omega = 50 \Omega, X_{in} = -2 \times 20 \Omega = -40 \Omega$$

(Z_{in} with X_{in} in series !)

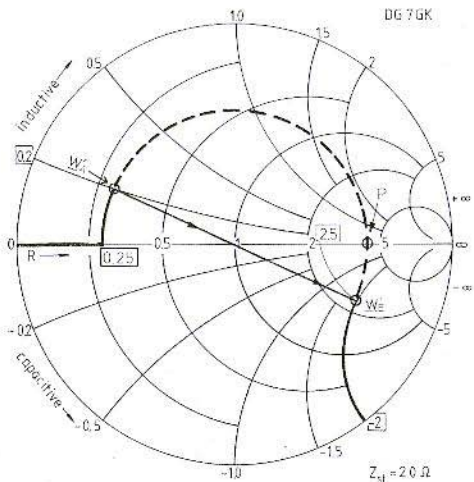


Fig. 2: Impedance transformation of W_{out} to W_{in} using a $\lambda/4$ line



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10 PRINT:PRINT:PRINT:PRINT
20 PRINT"EINGANGSIMPED. DES LAMBDA-VIERTEL-TRAFOS" :PRINT
30 PRINT"      BY G. STADLER":FORI=1TO2000:NEXT:PRINT"Q"
40 INPUT"GEBEN SIE WELLENWIDERSTAND EIN":Z:PRINT:PRINT
50 INPUT"GEBEN SIE ABSCHLUSS-WIRKWIDERSTAND EIN":RA:PRINT:PRINT:PRINT
60 INPUT"GEBEN SIE ABSCHLUSS-BLINDWIDERSTAND EIN":XA:PRINT"Q"
70 IF RA=0 AND XA=0 THENPRINT"      RE=UNENDLICH!":GOTO150
80 ZE=Z^2/(RA^2+XA^2)^(1/2)
90 IF RA<>0THEN GOTO 110
100 IF RA=0 THEN A=SGN(XA)*(PI/2):GOTO130
110 K=XA/RA
120 A=ATN(K)
130 PRINT"      RE="ZE*ICOS(A):PRINT:PRINT:PRINT
140 PRINT"      XE="(-1)*ZE*ISIN(A)
150 END
READY.

```

Fig. 3: BASIC program for calculation of the components of the input impedance of a $\lambda/4$ line as a function of the terminating impedance (impedance values in Ω , with input and output in numerical values)

NOTE: with respect to the previous example:

In certain circumstances, it may be advisable to make a semicircle in a clockwise direction from W_{out} (as shown in Figure 2 as a dashed line) around "1", instead of plotting a straight line: In this manner, it is also possible to determine point W_{in} . The semicircle forms the "transformation path" of the line! This means that if the line is shorter than $\lambda/4$, the transformation path will also be shorter than the semicircular arc. In this case, there is a proportional relationship between the length of the arc and line length. It is possible by selection of the line length to ensure that the transformation can, for instance, end on the horizontal axis of the Smith diagram. In the case of Figure 2, this corresponds to point P. In this case, the result will be that the input impedance is a pure real component: Point P is approximately 4.2, which when destandardized results in a Z_{in} of $4.2 \times 20 \Omega = 84 \Omega$. This would allow the power transistor to be well matched to a system with an impedance of 50Ω ($VSWR = 84 \Omega / 50 \Omega = 1.7$). It is, of course, possible to improve the matching still further by reducing the impedance of the stripline

(recommendation: repeat the above example with an impedance value of $Z = 15 \Omega$!).

Concentric circles in the Smith diagram replace a relatively complex calculation of the input impedance of a line. A BASIC program is shown in **Figure 3** in which the equation is programmed for the special case of a $\lambda/4$ line. The real and reactive impedances are inserted and result as numerical values in Ω . Attention should be paid that one lists capacitive reactive impedances with a minus sign. The program is, however, only suitable for series circuits. The same is valid, of course, when using the Smith diagram.

Since the accuracy of the computer is very often not required – possibly due to the tolerances of the impedances used – it may be of advantage to use the Smith diagram. This is also valid for applications in waveguide technology. It is then possible for reflection factors to be inserted into the diagram according to amount and angle. A standardization or destandardization is not required since the wave of a waveguide cannot be defined as of a specific impedance.

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Joachim Kestler, DK 1 OF

PLL-Oscillators with Delay Lines

Part 2: A Shortwave VFO from 5 to 6 MHz

4. A VFO FOR 5 TO 6 MHz

The basic fundamentals of PLL-oscillators equipped with delay lines were discussed in Edition 4/1984 of VHF COMMUNICATIONS. This article is to describe an easy to construct shortwave VFO, to allow readers to gain experience in this technology. Such a VFO can be used, for instance, as an oscillator in a 80 m/20 m receiver or transceiver, when using single conversion with a 9 MHz IF. Of course, the above mentioned frequency range is not fixed, and the module can be used anywhere in the frequency range from 2.5 to 7.5 MHz, (passband range of the delay line), which makes it also suitable for portable CW, and direct conversion receivers in the 80 and 40 m bands.

Even if you may not be interested in this frequency range, the material and time used is not lost, since the PC-board can be used for all other constructions to be described in this series without modification.

4.1. Circuit of the VFO

For clarity, the overall circuit diagram of the VFO

is split into three functional blocks. **Figure 16** shows the circuit diagram of the VCO with output stage and level control. The frequency-determining resonant circuit is formed from L1, C1, C2 and the tuning diodes D1 and D2. The signal path of the feedback loop is made via C4-T1-C9-T2-C5, and two dual-gate MOSFETs operating in class A are used as active components. These transistors have low-noise characteristics, and are also able to process sufficiently high signal power levels (see Part 1, Section 2.1.).

The output signal from the oscillator can be tapped off at the drain connection of T1, where it has no effect on the oscillator circuit. It is fed from there to the output stage I1. This is a multi-stage, integrated push-pull emitter follower with a voltage gain = 1, with a high input and a low output impedance that can be used up to approximately 40 MHz. This component offers a relatively high output power at low current drain (class B). A standard-level ring mixer (level: +7 dBm, impedance: 50 Ω) can be directly connected to the output of the VCO (Pt2 + R15); a second output (Pt3) is provided for the variable phase shifter.

An automatic gain control was provided in order to ensure a favorable and constant signal level within the circuit, and a clean sinewave signal at

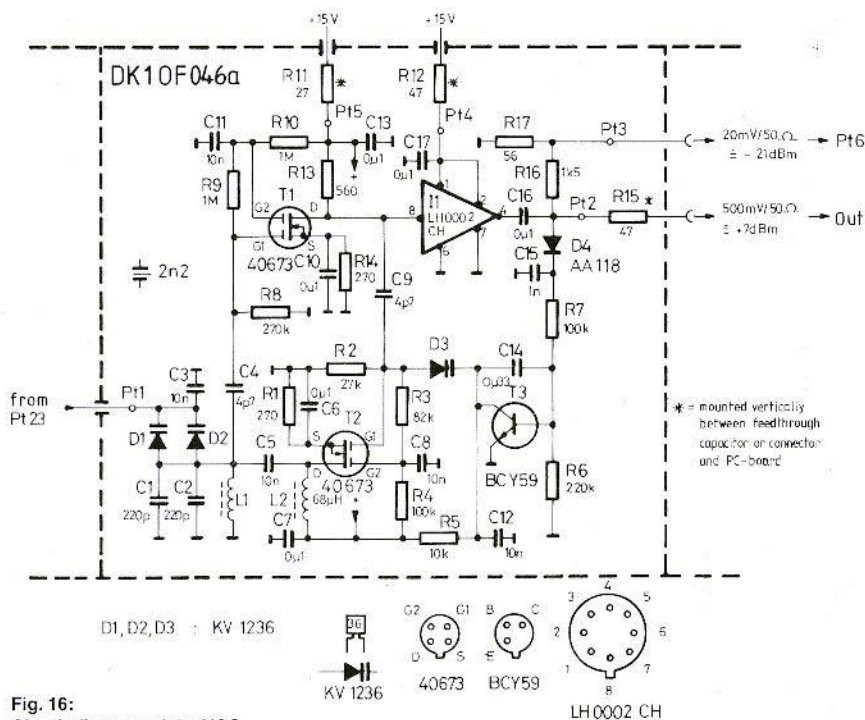


Fig. 16: Circuit diagram of the VCO

the output. Diode D4 generates a DC-voltage whose amplitude is proportional to the RF-voltage present at Pt2. Capacitor C9 and D3 form a variable voltage divider which allows the overall gain of the circuit to be adjusted so that the output level remains constant. Transistor T3 ensures the required voltage gain, which is necessary to obtain a sufficient slope for the control circuit.

The operating voltage for the output driver is fed in via Pt4; the VCO receives its carefully filtered operating voltage via the separate connection Pt5.

Hyperabrupt doted varactor diodes are used in this circuit; these diodes exhibit a large capacitance variation at a relatively low junction voltage range. The selected diodes were developed for use in AM-tuners of portable radio receivers (9 V supply) and are available inexpensively due to the large quantities produced.

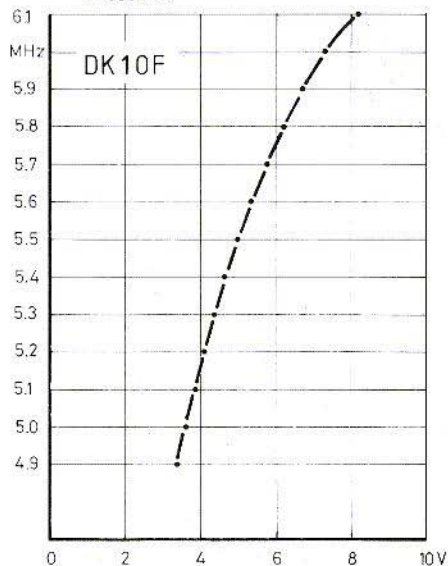


Fig. 17: Oscillator frequency of the VCO as a function of the tuning voltage

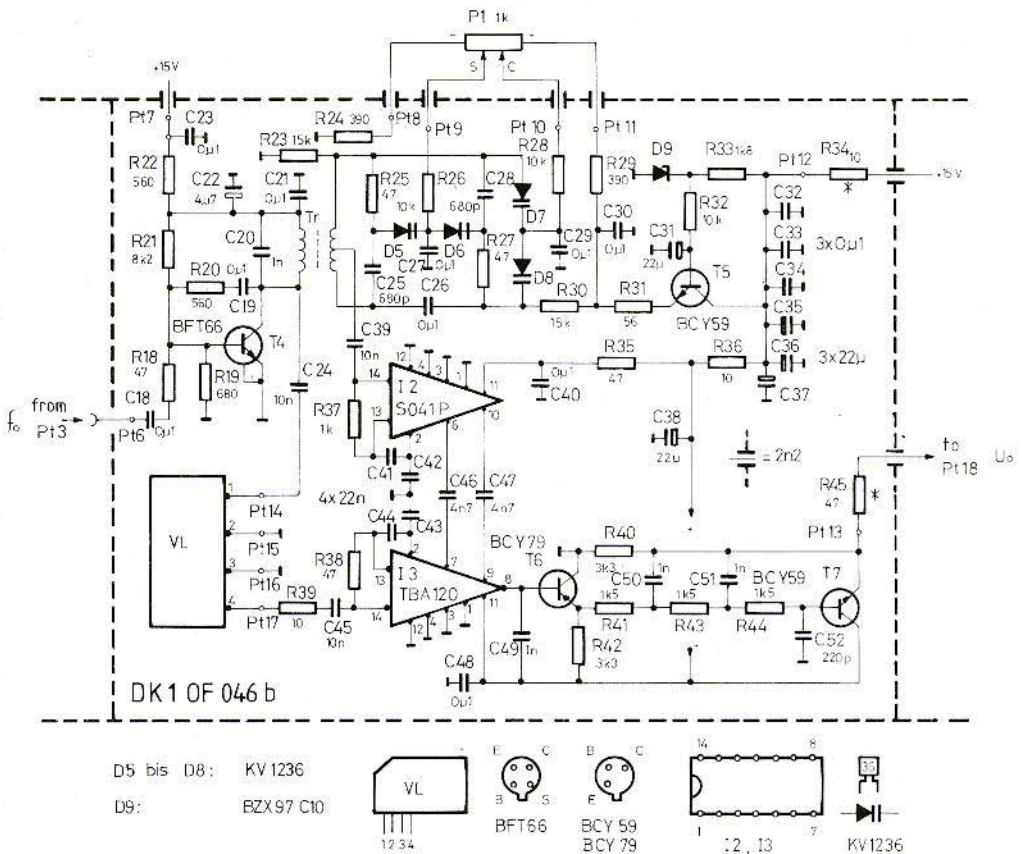


Fig. 18: Phase shifter, delay line and phase detector with filter

Figure 17 gives the oscillator frequency of the VCO as a function of the tuning voltage present at Pt1.

The next part of the circuit is shown in Figure 18. The VCO signal from Pt3 is fed via Pt6 to an amplifier stage equipped with transistor T4. This stage is provided with feedback (R20, C19) so that it is possible for transformer Tr to be fed at low impedance, and is thus able to exhibit a flat frequency response. The operation and circuit of the variable phase shifter was described in detail in Part 1 of this article. The stabilizer stage equipped with T5 and D9 ensures that the diode voltages have a low hum and noise level.

The sine-cosine potentiometer P1 is used for tuning. It is supplied via P18 and P11; P9 is connected with "S" (sine), and P10 with "C" (cosine). Connection "E" remains disconnected. The tuning direction can be inverted by changing S and C (rotating to the right → lower frequency).

The delay line VL receives its input signal from T4 via C24 and Pt14. Its output is fed via Pt17, R39, and C45 to the input of a limiting amplifier I3 (TBA 120). This limiting process means that the pass-band curve of the delay line no longer has an effect on the parameters of the circuit, as long as the

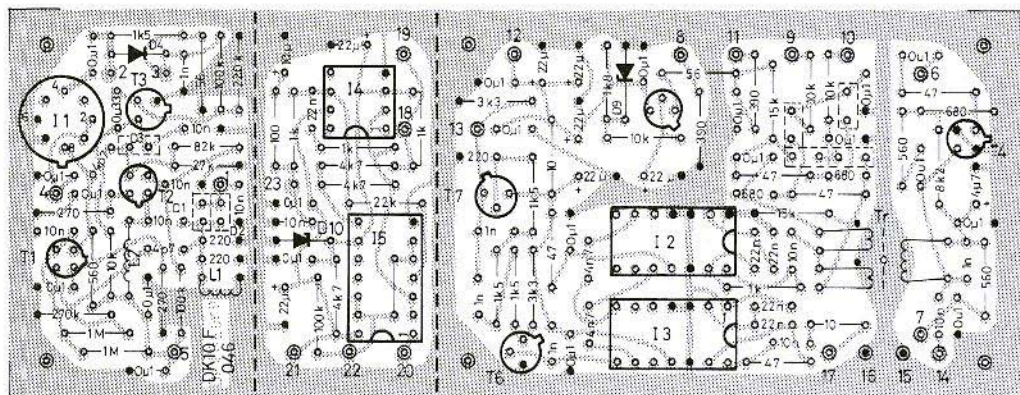


Fig. 20: Component locations on the VFO PC-board DK10F 046

Integrated circuit I5 can be classed as a remotely controlled analog switch. If contact S1 connected to Pt22 is closed, this will open the "contacts" designated 1-2, 3-4, and 8-9. If S1 is open, this will close the three analog switches: 8-9 will close (via R49) and short the input signal; 3-4 will discharge the integration capacitor and will convert I4 to a proportional amplifier, and finally 1-2 will connect potentiometer P3 to the input of the operational amplifier via Pt20 and R48. In this condition, the VFO can be directly tuned via P3 to enable rapid frequency changes; a closing of switch S1 ensures that the circuit will be synchronized to the nearest lock-in point (maximum deviation: ± 7.8125 kHz). The tuning is then once again made by P1.

4.2. Construction

PC-board DK10F 046 has been designed for accommodating the described circuit. This board is single-coated and its dimensions are 135 mm x 50 mm. It is suitable for mounting in a standard metal box. The component locations are given in Figure 20.

The mechanical work is commenced by making the holes in the side panels for the feedthrough capacitors (Pt4, 5, 7, 8, 9, 10, 11, 12, 19, 20, 21, 22), for the RF-connectors and feedthroughs (Pt2, 3, 6). This is followed by filing the PC-board (without components) to fit into the case, after which it is soldered into position with a spacing of 6 mm between board and lower edge of the case. This is followed by installing the two screening panels with feedthrough capacitors between Pt1 and Pt23, and between Pt13 and Pt18. These screening panels are shown as dashed lines in Figure 20. Resistors R11, 12, 15, 34, 45, 46, 47, and 48 are mounted vertically between the PC-board and the feedthrough capacitors or RF-connector.

It is now possible for the other components to be mounted into place on the board. Sockets can be used for the integrated circuits (with the exception of I1); do not forget the wire bridge below I5! Figure 21 shows a photograph of the completed prototype.

The delay line is placed over the other components of this part of the circuit so that short connections can be made to Pt14 to Pt17. A piece of foam is placed between the cover and the delay line to hold it in position.

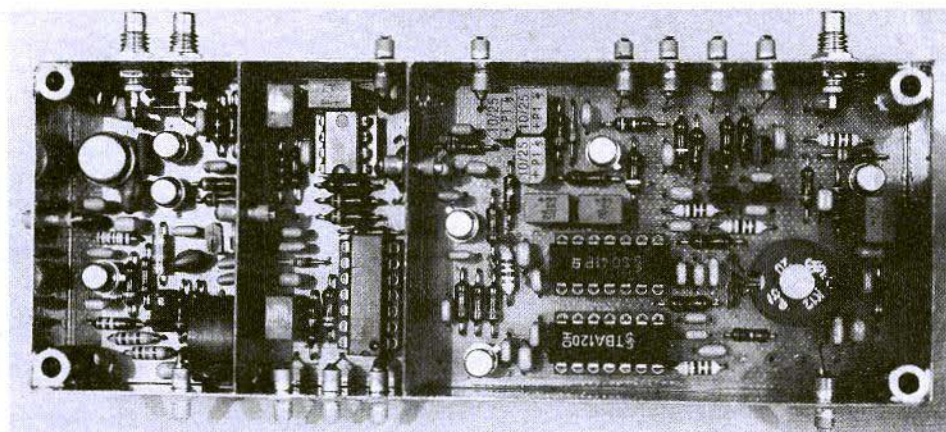


Fig. 21: Photograph of the author's prototype using SMC-connectors, and bushings for screwing the cover and the module into place

Special Components

- | | | | |
|-----------------------------|---|-----------------------|--|
| I 1 : | LH0002CH
(National Semiconductor) | C57 : | Tantalum electrolytic 10 μ F/25V,
for vertical mounting,
spacing 5 mm |
| I 2 : | SO41P (Siemens)
or TBA120 | All other capacitors: | Ceramic disk types 30 V DC.
Spacing for all resistors: at least 7.5 mm |
| I 3 : | TBA120
(various manufacturers) | L 1 : | Siemens potted core 14 x 8,
material K12, AL = 20
Order No. B65541-K0020-A012;
coil former: Order No.
B65542-A0000-M002 (2 cham-
bers).
9 turns of 0.25mm silver plated,
insulated copper wire,
glue the two halves and winding
with epoxy paste. |
| I 4 : | LF356N (Siemens)
or LF356H | L 2 : | Ferrite choke 68 μ H |
| I 5 : | CMOS4066B
(various manufacturers) | Tr : | Core and coil former as L 1
primary: 8 turns of 0.3 mm dia.
enamelled copper wire (in one
chamber), sec.: 2x4 turns of
0.3mm dia. enamelled copper
wire, wound in a bifilar manner
(in the other chamber) |
| T1, T2 : | 40673 or 40841 (RCA) | VL : | PAL delay line, e.g. DL-700
(Philips) |
| T3, T5, T7 : | BCY59, BC109, BC413, BC550
or similar NPN transistor | P 1 : | Sine-Cosine potentiometer
1k Ω , type SCX50 (MEGATRON,
D-8011 Putzbrunn
Tel.: FRG-89-463021) |
| T4 : | BFT66 (Siemens) | P 2, P 3 : | Potentiometer
10k Ω /0.25W, linear |
| T6 : | BCY79, BC179, BC415, BC560
or similar PNP transistor | | |
| D1,2,3,5,6,7,8 : | KV 1236
(Componex GmbH, Düsseldorf) | | |
| D4 : | AA 118 or similar Ge-diode | | |
| D9 : | BZX97C10
or other 10 V zener diode | | |
| D10 : | BZX97C6V8
or other 6.8V zener diode | | |
| C22 : | Tantalum electrolytic 4.7 μ F/35V
for vertical mounting,
spacing 5 mm | | |
| C31,35,36,37,
38,53,59 : | Tantalum electrolytic 22 μ F/16V,
for vertical mounting,
spacing 5 mm | | |



4.3. Commissioning

Firstly examine the VCO. This is achieved by connecting the operating voltage of + 15 V to Pt4 and Pt5 (via R11 or R12), and providing a variable bias voltage of 0 to - 10 V to Pt1 (after disconnecting it from Pt23). This bias voltage can be taken via a potentiometer of approximately 10 k Ω from the 15 V operating voltage. Connect output (Pt2 via R15) to a frequency counter (use the 50 Ω input or connect an additional terminating resistor).

It is now possible for the tuning curve to be determined and compared with Figure 17. Deviations of 10 % at the lower and 20 % at the upper end of the range are permissible, and corrections can be made by varying C1 or C2.

If the oscillator does not commence oscillation, firstly check the voltage drop across the source resistors of T1 and T2 (test point: transistor case). Voltages of between + 2 V and + 3 V should be present here. If the measured voltages differ greatly from this, replace these transistors. If no oscillation is determined although the voltages are correct, increase the value of C9 experimentally to approximately 20 pF. A DC-voltage of between + 3 V and + 6 V should be present at the collector of T3 (test point: transistor case); it can be varied with the aid of C9.

If a suitable oscilloscope is available (bandwidth \geq 20 MHz), it is possible to use this to analyze the output signal with respect to level and sinewave form (do not forget the 50 Ω termination at the output).

If the VFO is only to be used for a reduced frequency range (e.g. only from 5 to 5.5 MHz), it is recommended that this range is spread over the whole tuning voltage range (see Part 1, Section 2.1.). This can be achieved by replacing one of the two tuning diodes (D1 or D2) by a fixed capacitor of the required value.

Now, connect the tuning potentiometer P1 experimentally via Pt8 to Pt11 to the circuit, and connect Pt3 and Pt6 with the aid of a piece of coaxial cable. After connecting also Pt7 and Pt12 to the supply voltage, check the DC-voltage level at the interconnection point of R21 and R22. A voltage of + 9 V should be measured at this point (permissible tolerance: + 1 V, correct via R21).

The voltmeter is now connected to Pt13 (or to the feedthrough capacitor to R45) and the temporary tuning voltage at Pt1 adjusted so that the oscillator operates approximately at the center of the band. P1 is now rotated and the voltage measured at Pt13 will vary periodically between a minimum and maximum value. The minimum should not be more than + 5 V, and the maximum not less than + 9 V. The following was measured on the author's prototype: $U_{\min} = + 4$ V, $U_{\max} = + 13$ V. Otherwise, I3 will not be operating correctly (caution should be paid when purchasing super components whose quality is not known).

The voltage at Pt13 will vary with time when the control loop is open, which is the result of the normal free-running instability of the VCO. However, it should vary continuously when rotating P1 slowly, and should not jump. The latter would indicate self-oscillation in the VCO.

Finally, remove the variable bias voltage from Pt1, and connect this point to Pt23. Potentiometers P2 and P3, and switch S1 are temporarily connected. After connecting + 15 V again to Pt21, the oscillator should be tunable over the whole range with P3 after opening switch S1.

The closing of S1 allows the circuit to lock in at the nearest lock-in point. This is a maximum of ± 8 kHz from the selected free-running frequency. If

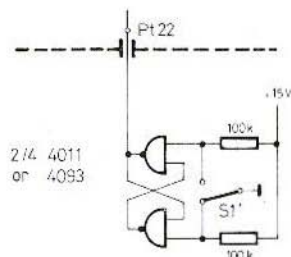


Fig. 22: Suppressing contact bounce of switch S 1

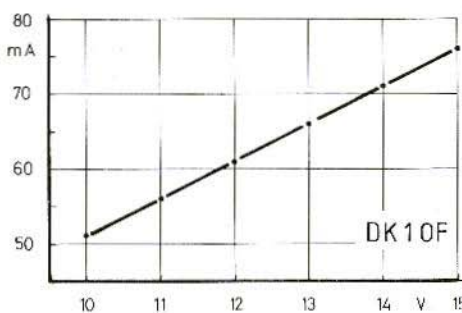


Fig. 23: Overall current drain as a function of the operating voltage

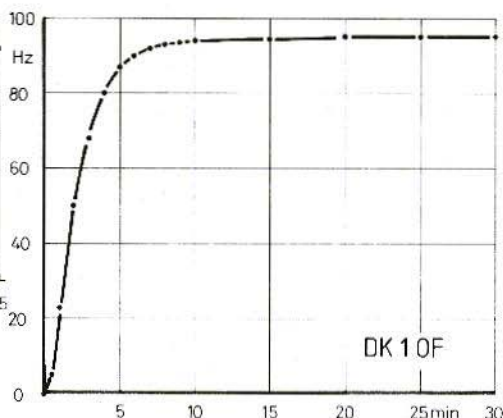


Fig. 24: Transient drift of the oscillator

large jumps result on switching, this would indicate a mechanical bounce of S1. This can be suppressed by using a switch with change-over contact and two CMOS gates for suppression; such a circuit is shown in **Figure 22**. It should be noted when using CMOS chips that unused inputs cannot be left disconnected, but must be either grounded or connected to the operating voltage.

A stable, well-filtered operating voltage is required for supplying the oscillator; this can be obtained, for instance, using a fixed voltage stabilizer (7815). This stabilizer should not be used to supply other modules, whose current drain varies considerably (e.g. AF-amplifiers). It is recommended that the operating voltage for the VCO (Pt5) is fed via an additional filter link (series resistor

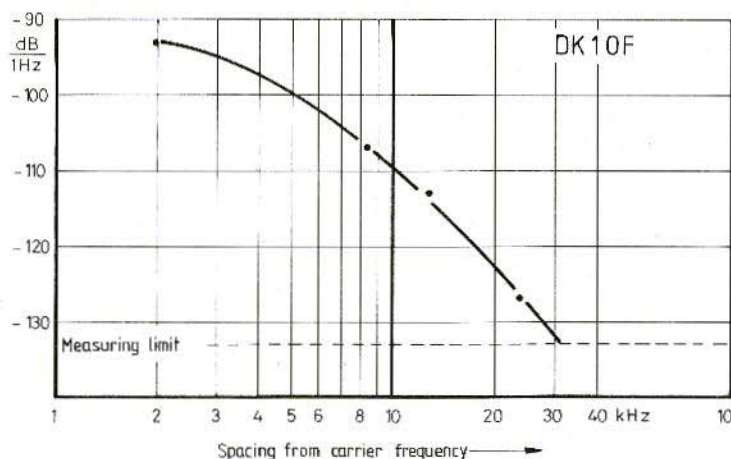


Fig. 25: Wideband noise after doubling the frequency to 10.7 MHz



22 Ω , together with a 1000 μF electrolytic to ground).

The value of the operating voltage is not very critical. The circuit will operate even with 10 V, which could be of interest for portable operation (12 V accumulator and stabilizer). The overall current drain as a function of the operating voltage is given in **Figure 23**.

4.4. Measured Values

The values given in the following tables were measured at an operating voltage of 15.0 V, and a constant ambient temperature of 22°C.

Frequency range: 5 to 6 MHz
Output level: -7 dBm Δ 500 mV into 50 Ω

Current drain: 76 mA
Frequency drift: < 100 Hz, in the first 10 minutes, afterwards < 10 Hz per hour (**Figure 24**)
Harmonic rejection: > 30 dB
Spurious signals: none
Sideband noise: see **Figure 25**
Sensitivity to voltage fluctuations: - 400 Hz/V

A highly selective IF-amplifier with 3 crystal filters at 10.7 MHz and subsequent RMS-voltmeter was used for measuring the sideband noise. It was necessary during these measurements for the oscillator frequency to be doubled (RK-2 from MCL). The actual noise values are therefore most certainly better than those given in **Figure 25**.

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SO 239	0321	DM 199,—
N	0322	DM 217,—





Manfred Mühlbacher, DB 9 SB

A 2.3 GHz Prescaler (: 100)

New, inexpensive integrated preamplifier and divider circuits allow direct frequency measurements to be made up to and in excess of the 13 cm band, and led to the design of the prescaler described in this article. The designation "inexpensive" does not necessarily mean that they are cheap: The required ICs are most certainly worth their price, but are not cheap for us radio amateurs! The subsequent frequency counter needs only to have a cutoff frequency of 25 MHz, and should have a good time base!

1. PRESCALER CONCEPT

The block diagram of the prescaler is shown in **Figure 1**. It is provided with a PIN diode attenuator at the input, and two preamplifiers. This is followed by the fast 2:1 divider. Half the input frequency

is usually too weak in order to drive the 10:1 divider SP 8668 B (Plessey), and for this reason, a 20 dB intermediate amplifier is provided. A subsequent 5:1 divider then brings the overall frequency division ratio to 100:1. The input frequency divided by 100 is now available at ECL-II level. If TTL-level is required, this can be achieved by providing a converter stage using an AF or switching transistor and a Schottky gate. This will generate steep impulses at TTL-level, that can be processed in any subsequent frequency counter having a band width of at least 25 MHz. An offset voltage as described in (1) is not to be expected.

The components within the dashed lines: the electronic attenuator, and the first preamplifier, can be deleted or provided later. **Figure 2** shows the prescaler equipped in this manner.

1.1. Electronic Attenuator

In order to increase the dynamic range of the prescaler, it was provided with a voltage-controlled PIN diode attenuator type UTF-025 manufac-

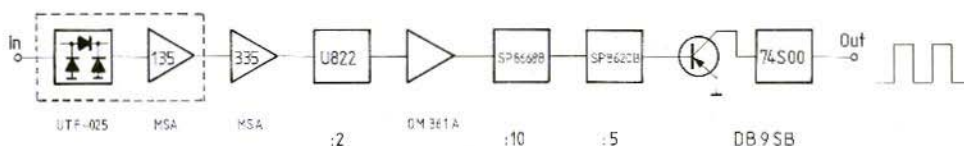


Fig. 1: Block diagram of the 2.3 GHz divide-by-100 prescaler

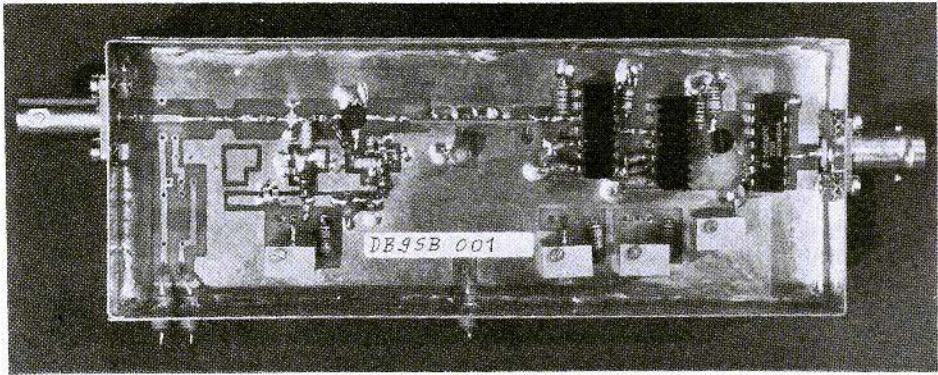


Fig. 2: In this prototype, the author has deleted the PIN diode attenuator and the first preamplifier

tured by Avantek. It operates in the frequency range of 5 to 2500 MHz. Its input and output impedance is 50Ω . The maximum attenuation amounts to 40 dB at 10 MHz, approx. 25 dB at 1 GHz, and 20 dB from approximately 2 GHz up. The maximum permissible input power amounts to +23 dBm, which corresponds to 200 mW or 3.1 V into 50Ω . At a price of approximately 100 US-Dollar (Summer 1984), this PIN attenuator is only a quarter of the price of a mechanical attenuator. The connections of this component are shown in Figure 3. Since the prescaler is very sensitive, attention should be paid that the input power at 2300 MHz should never be more than 1 to 2 mW, corresponding to 0.223 V into 50Ω . May be one of our readers has a useful recommendation how this attenuator can be automatically controlled by the input signal.

1.2. Preamplifier

At present, two main types of internally matched amplifiers are suitable for use with an operating voltage of 5 V: The GaAs-FET types CGY manufactured by Siemens, and the monolithic silicon amplifier (MSA)-types manufactured by Avantek. The latter provide a far better value for money, and are therefore used in the following description. Construction is not critical if the information

given in the description is observed. The number of amplifiers that were destroyed during the development could be limited to four.

The case and the basic circuit of the Avantek-MSA amplifiers are shown in Figure 4. The other types given in Table 1 mainly differ from each other in their higher output levels.

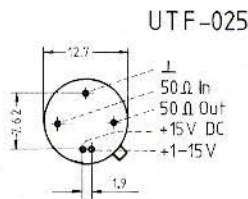


Fig. 3: The electronic attenuator UTF-025

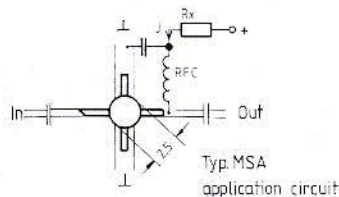


Fig. 4: Monolithic microwave amplifier manufactured by Avantek



Type	U_B	Gain (2.4 GHz)	P_{out} (25 °C)	Current *	Usable to GHz/Gain
MSA 0135/21	5.2 V	12.00 dB	1.8 dBm	17 mA	4 GHz / 7.2 dB
MSA 0235/21	5.2 V	10.40 dB	3.5 dBm	25 mA	4 GHz / 6 dB
MSA 0335/21	5.2 V	10.70 dB	11.0 dBm	35 mA	4 GHz / 6.8 dB
MSA 0420/21	6.5 V	7.53 dB	17.8 dBm	90 mA	4 GHz / 4 dB
MSA 0435/21	5.5 V	7.30 dB	13.2 dBm	50 mA	4 GHz / 4 dB
MSA 0470/21	5.5 V	7.56 dB	13.2 dBm	50 mA	4 GHz / 4 dB

Table 1

*Since these are "Shunt-feedback" amplifiers, it is necessary to observe the given currents for maximum gain. The voltage should also be set as exactly as possible. In this manner, a series circuit comprising the MSA 0135 and MSA 0335 will provide a gain of approximately 30 dB up to 1 GHz, which drops continuously to 20 dB up to 2.6 GHz. If no care is made with the currents, this can cause a loss of gain of up to 10 dB in the cascade circuit.

Avantek has mentioned that the MSA types will be available in a cheaper case in the near future with prices in the order of 10 US- $\$$.

1.3. Frequency Dividers

A frequency divider type U 822 manufactured by Telefunken is used as 2.3 GHz-divider. It divides the input frequency by 2. This IC is selected at 2.3 GHz in the factory. It was mainly developed for use for the first IF of future satellite TV-receivers. Later, due to the high quantities involved, the price should finally drop to approximately 20 US- $\$$. **Figure 5** shows the case and connections of this integrated divider type U 822 BS.

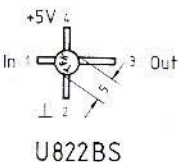


Fig. 5:
The divide-by-two
prescaler up to 2.3 GHz
manufactured by
Telefunken

The divide-by-two module U 822 is followed by a divide-by-ten IC manufactured by Plessey, which is designated SP 8668 B, that operates up to 1.5 GHz. It requires an input voltage of approximately 400 mV (peak-to-peak) to operate reliably. Since the output voltage of the U 822 at an input frequency of 2320 MHz only amounts to approximately 70 mV (peak-to-peak), it is necessary for an intermediate amplifier to be provided using the inexpensive OM 361 A. Telefunken has stated that a new divider with a higher output voltage will be produced at a later date. In this case, it will be possible for the intermediate amplifier to be deleted.

The subsequent divide-by-five IC type SP 8620 B manufactured by Plessey increases the overall division ratio to 100.

Further notes regarding the use of other frequency dividers with differing division ratios are to be mentioned in Section 7.

2. OVERALL CIRCUIT DIAGRAM

The complete circuit diagram of the 2.3 GHz prescaler module is given in **Figure 6**. The amplifier and frequency dividers will only operate reliably when the given voltages and currents are maintained. For this reason, all voltages should be individually stabilized electronically and be exactly adjustable with the aid of multi-turn trimmer potentiometers. It is possible for the voltages to be slightly increased during the alignment process in order to find the most favorable value.

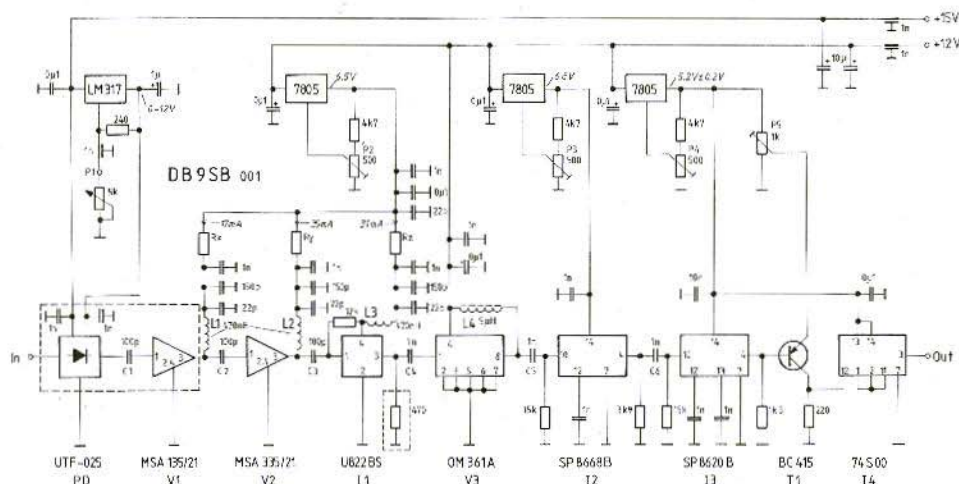


Fig. 6: One will notice several chokes and extensive bypass of the microwave dividers and amplifiers in the overall circuit diagram of the 2.3 GHz prescaler

Unfortunately, the PIN diode attenuator requires an operating voltage of 15 V. The variable DC-voltage for adjusting the attenuation (P 1, LM 317) is derived from this voltage. Figure 7 shows the connections of this voltage stabilizer.

The 470 Ω resistor within the dashed lines at the output of the divide-by-two IC I1 originates from a suggestion by HB9MIN: The resistor increases the output voltage of the U 822 by approximately 8 dB. Since this is still not sufficient for driving the SP 8668, it is possible for this resistor to be deleted.

2.1. Special Components

PD: UTF-025 (Avantek)
V 1: MSA 0135/21 (Avantek)

V 2: MSA 0335/21 (Avantek)
V 3: OM 361 A (Philips)
I 1: U 822 BS (Telefunken Electronic)
I 2: SP 8668 B (Plessey)
I 3: SP 8620 (Plessey)
I 4: 74 S 00
T 1: BC 415, BC 560 or similar PNP transistor

L 1 – L 3: 0.47 μ H miniature choke
L 4: 4.7 μ H miniature choke
C 1 – C 3: 100 pF miniature chip capacitor (ATC or similar)
C 4 – C 6: 1 nF miniature chip capacitor (ATC or similar)

Other bypass capacitors:

Ceramic disk, or miniature chip capacitors:
3 ceramic feedthrough capacitors 1 – 2 nF, for solder mounting;
Polarized capacitors: Tantalum electrolytics (bead type);
4 trimmer potentiometers, for vertical mounting, 10 x 5, spacing 5 x 2.5 mm;
2 heat sinks for DIL 14;
1 metal case 148 x 56 x 30 mm;
3 voltage stabilizers 7805;
1 voltage stabilizer LM 317.

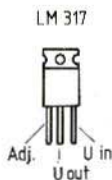


Fig. 7: Voltage stabilizer LM 317 for the UTF-025

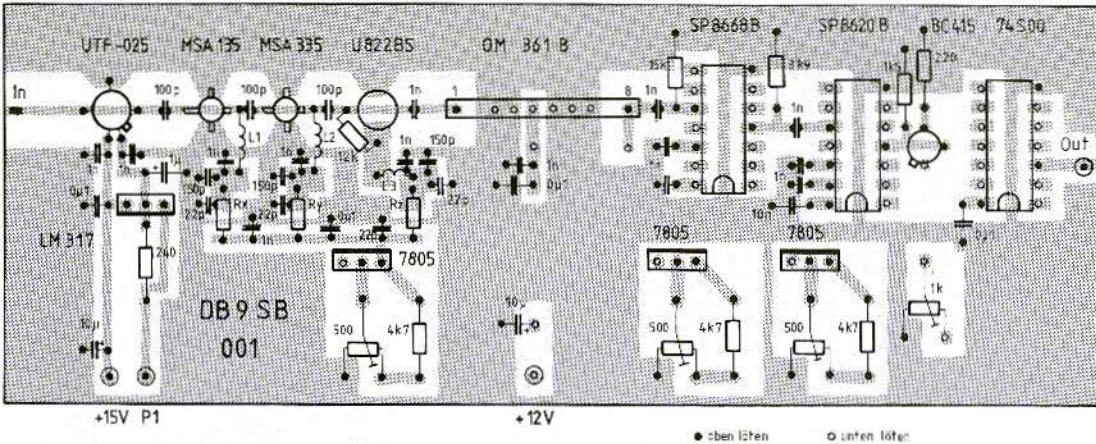


Fig. 8: Component locations on the double-coated PC-board DB9SB 001; the other side of the board is also provided with conductor lanes

3. CONSTRUCTION

The circuit diagram given in Figure 6 can be accommodated on PC-board DB9SB 001, which is shown in Figure 8. This board is double-coated, but without through-contacts. The material used is epoxy glassfibre with a thickness of 0.8 mm. The first prototypes were made on RT/duroid with a thickness of 0.79 mm, however, the epoxy ma-

terial did not cause practically any deterioration of the sensitivity after changing the conductor lane width to 1.37 mm for 50 Ω. The price difference when using a board of 146 x 54 mm is considerable!

A coaxial connector suitable for SHF must be used at the input of the divider, preferably using a flange type. The PC-board is soldered around the edges on both sides so that the same spacing is provided above and below the board. The four voltage stabilizers, their bypass capacitors, and

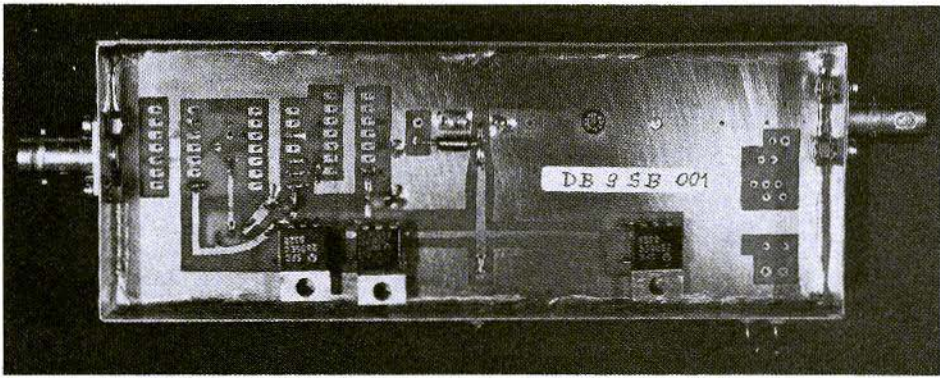


Fig. 9: Lower side of the author's prototype (without attenuator and first preamplifier)

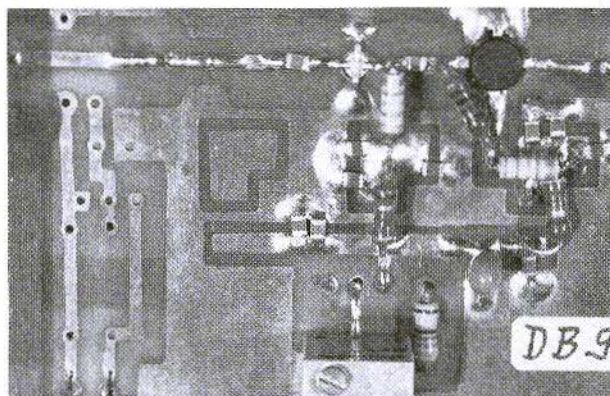


Fig. 10:
Close-up of the input circuit

choke L 4 are soldered into place on the lower side of the board, which is the side marked with the author's call sign. The voltage stabilizers are then bent back as shown in **Figure 9**.

The conductor lane cutouts for PD and C 1 can be cut with the aid of a sharp knife – approximately 6 mm is required for the attenuator and 1 mm for the chip capacitor. The 50 Ω line is provided as a continuous line, in order to allow the prescaler to be used without PIN diode attenuator and preamplifier.

The miniature chip capacitors can be mounted easily if one's eyes are good, or when a magnifying glass is used. The wire ends of the bypass capacitors must, however, be as short as possible, especially those used in conjunction with the Plessey ICs. Suitable holes are drilled in the PC-board for the Avantek preamplifiers and the Tele-

funken divide-by-two prescaler. These components are placed onto the board with the markings facing downwards into the PC-board. This can be seen in more detail in **Figure 10**.

4. ALIGNMENT

The PC-board can be completely equipped with the exception of capacitors C 4 and C 5. All trimmer potentiometers should be adjusted to their fully anticlockwise position.

The voltages and currents given in **Table 2** should be adjusted after connecting the operating voltage(s).

Potentiometer	Act. comp.	Current	Voltage (V)
P4	I3 und I4	–	5,2 ± 0,2
P3	I2	–	6,8 ± 0,3
P2	V1, V2, I1	–	6,5
R _x	V1	17	–
R _y	V2	35	–
R _z	I1	31	ca. 5

Table 2



The author used metal-film types for the dropper resistors.

This is followed by connecting the output of the prescaler via a short coaxial cable to an oscilloscope with a bandwidth of at least 25 MHz. Firstly examine I 3 for any tendency to self-oscillation. This is done by rotating P 5 in a clockwise direction until approximately 5 V (TTL-high) is present at the output, switching the oscilloscope to AC-voltage coupling, and to a sensitivity of 100 mV/div. If P 5 is rotated further, and if sinewave oscillations are noticed, this will indicate that I 3 is oscillating and it will be necessary to connect 15 k Ω between pin 10 of I 3 and ground (below).

After soldering C 5 into position, one will immediately notice whether I 2 breaks into oscillation. Until now, every SP 8668 B used by the author has broken into oscillation! 15 k Ω at the input is all that is required for neutralization.

The preamplifier OM 361 A will not break into oscillation – in contrast to its predecessor, the OM 361. I 1, on the other hand, will oscillate at the fre-

quency of its highest sensitivity, which is at approximately 1.4 GHz. It is necessary here to provide a resistor of approximately 12 k Ω between input and +5 V, that is between pins 1 and 4 of the U 822 BS.

No tendency to self-oscillation was noticed in the case of the preamplifiers. The oscilloscope image should now be free of amplitude variations when rotating P 5 slowly through its range.

If an oscillator with an output power of 1 mW in a frequency range of between 1000 and 1500 MHz is fed to the prescaler, a virtually square-wave TTL signal will appear on the oscilloscope on rotating P 5. The prescaler is now connected to a counter, and P 5 adjusted so that the counter provides a stable reading. This completes the alignment.

The given frequency range was selected since the dynamic range of the module is greatest in this range, as can be seen in **Figure 11**. The dynamic range is considerably less in the 13 cm band at 2320 BS, which means that it is necessary to

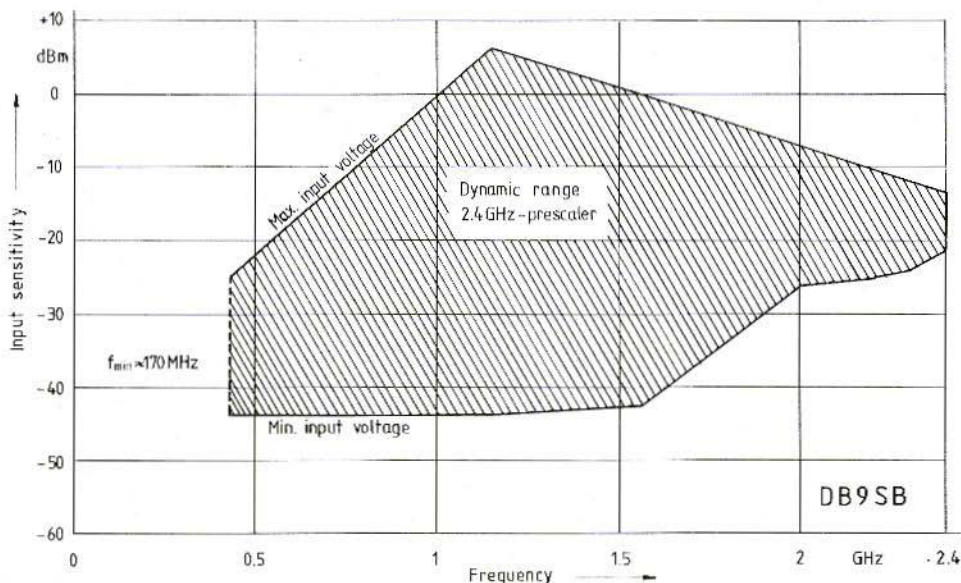


Fig. 11: The input signal to be measured must be within the shaded area

use a preamplifier and to adjust the PIN diode attenuator in order to obtain a stable reading.

The operating current of the complete prescaler module is in the order of approximately 320 mA.

5. NOTES

It has been found that I 1 works best when the power at the input of the first divider is between 0 and +5 dBm. If the module is used without PIN diode attenuator, it is necessary to ensure with the aid of suitable attenuators (fixed or variable) that the input power is not too high. If it is in excess of the dynamic range (see Figure 11), a reading of 000 will be indicated.

The highest operating frequency measured on the author's prototype was 2430 MHz without cooling, and approximately 2.6 GHz when I 1 was cooled. The lower frequency limit is in the order of 140 to 170 MHz. The author would like to point out, however, that his U 822 was selected in a Telefunken laboratory at 2400 MHz. Those available on the market are, on the other hand, automatically measured at 2300 MHz.

For the first time, it is now possible for radio amateurs to measure frequencies up to 2.3 GHz. At present, there are no commercially available counters on the market that can measure this very high frequency directly! Of course, this high technology has its price: When fully equipped, the components used in the prescaler module alone will have a value of approximately 900.—DM. Even without PIN diode attenuator and first preamplifier, it will still be approximately 500.—DM. However, the high value is relative when one considers that a commercial prescaler of this type would most certainly cost many times this price. In addition to this, suitable measuring equipment is becoming more and more important, the higher one goes in the microwave range.

The author hopes that he has been able to bridge a gap, and will be only too pleased to assist interested readers in obtaining some of the components. At present, the author is working on a new frequency counter which should be able to count up to 2.5 GHz. It will have 9 digits and the frequen-

cy should be indicated after a measuring period of 0.4 s. A special feature is a switchable time base, which allows one to use prescalers with a non-decadic division ratio in the future. If this frequency counter is of interest to our readers, the author will be only too pleased to write an article on it.

6. REFERENCES

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- 2) Telefunken-Electronic, Heilbronn: Datenblätter U822BS, U824BS
- 3) AvanteK: Cascadable Monolithic Silicon Integrated Amplifier
- 4) Plessey: High-Speed Dividers Handbook, SP8000 Series
- 5) E. Zimmermann, HB9MIN: 2.5 GHz-Teiler Tagungsheft der VHF/UHF 1984 München
- 6) Das TTL-Kochbuch, Texas Instruments
- 7) H. Mazur, DL6WA: Einfacher Vorteiler für Frequenzen bis über 1 GHz mit Dezimalisierung des Teilfaktors cq-DL 2/1983, page 62—63

7. POSSIBLE MODIFICATIONS

At present, three different prescalers are known to the author for frequencies over 2 GHz:

U 822 BS	2.3 GHz	÷ 2	Telefunken
U 824 BS	2.3 GHz	÷ 4	Telefunken
SP 8712	2.5 GHz	÷ 4	Plessey

If one wishes, it is possible to use the following dividers subsequently: U 624 (÷ 64), or U 626 BS (÷ 256). The advantage is that both possess a built-in preamplifier. The disadvantage is the non-decadic division ratio which must be further divided according to (7) in order to achieve a total frequency division of 1000.

If one knows the internal circuitry of one's counter well enough, it is possible for the time base to also be modified. This, on the other hand, also has its effects on the other prescalers already built in. The most elegant way would therefore be to provide an additional board behind

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each DM 39.50

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Double coated, drilled PC-board, 2 GaAs-FETs,
2 Si-FETs, 3 transistors, 3 diodes, 2 volt. regulat.,
3 Neosid coils, 4 RFCs, 2 special mini ferrite beads,
9 green and 2 black mini foil trimmers, trapez. caps:
3 x 10p and 1 x 47p, 2 stripline chip caps., 7 ceram.
and 13 decoupling caps., 2 tantalum electrol., 17
resistors, 1 trimmer pot., 2 crystals, 3 feed-throughs,
2 N-sockets with plane BNC flange, 1 drilled tinned-
metal box, 1 piece of conductive foam

Additional set of parts for open-air use of converter:

1 plastic box, 1 plastic mounting plate, 1 thermo
switch, 1 heater resistor, 1 DIN socket

6918 DM 110.—

Converter ready-to-operate in tinned-metal box

6919 DM 582.—

Converter ready-to-operate in weather-proof box

3027 DM 692.—

DL6NAD	Multiple Digital Image Storage for WEFAX Images		Ed.	1/1985
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PC-board DL6NAD 001 double coated, with through contacts

6913 DM 68.—

PC-board DL6NAD 002 double coated, with through contacts

6914 DM 69.—

Components DL6NAD 001/002:

6915 DM 625.—

1 RAM, 24 D-RAMs, 7 TTL-ICs, 1 EPROM, 11 CMOS-ICs
1 lin. IC, 1 diode, 2 connector strips 2x20 pins,
1 connector strip 2x8 pins, 1 IC socket 28 poles,
1 socket 14 poles, 1 DIL switch, 24 capacitors, 10
tantalum electrol., 2 aluminium electrol., 7 solder
pins, 33 resistors.

Kit DL6NAD 001/002 complete, with above components

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YU3UMV 003 Colour Module with Composite Output

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Ed. 1/1985

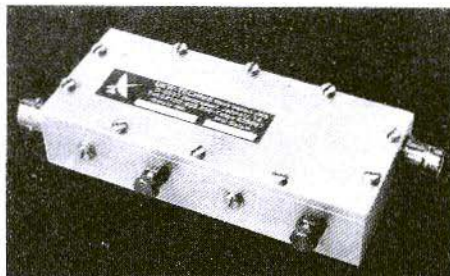
No PC-boards or components available

DK10F	Shortwave VFO from 5 to 6 MHz	Art.No.	Ed.	1/1985
PC-board	DK10F 046 single-coated, silver-plated, drilled, with component location plan	6891	DM	27.-
Semiconductors	DK10F 046 5 ICs, 7 transistors, 10 diodes	6897	DM	145.-
Components	DK10F 046 2 potted-core sets, 1 m copper wire, 1 mini RFC, 1 PAL delay line, 2 trimmer potentiometers, 9 tantalum electrolytics, 12 feedthrough and 50 ceramic caps., 57 resistors, 1 tinned metal box	6892	DM	105.-
Kit	DK10F 046 with the above parts, i.e. without sin-cos-potentiometer	6893	DM	268.-
DB9SB	2.3 GHz Prescaler	Ed.	1/1985	
PC-board	DB9SB 001 double-coated, silver-plated, undrilled, without component location plan	6894	DM	21.-
Components	DB9SB 001 1 off U822BS, 74S00, BC415 each, 3 off 7805, 1 tinned-metal-box, 2 BNC flange sockets, 4 mini RFCs, 3 feedthrough and 22 ceram. caps., 6 chip capacitors, 7 tantalum electrolytics	6895	DM	145.-
Kit DB9SB 001 with the above parts, i.e. without UTF, MSA, OM..		6896	DM	160.-

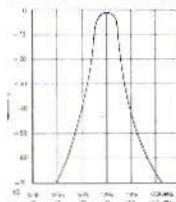
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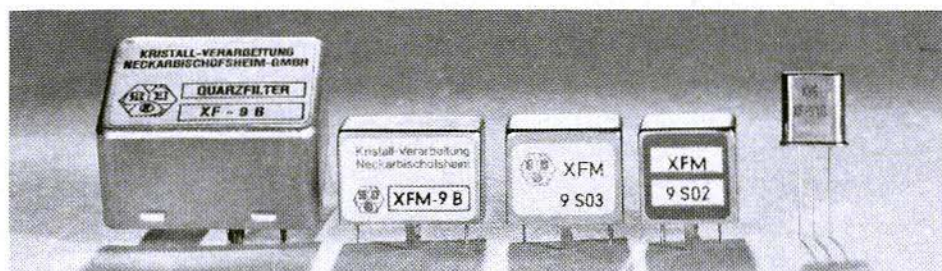
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XF-9B	SSB	XFM-9B	500 Ω 30 pF	15	XFM-9S03	1.8 kΩ 3 pF	14
XF-9C	AM	XFM-9C	500 Ω 30 pF	15	XFM-9S04	2.7 kΩ 2 pF	14
XF-9D	AM	XFM-9D	500 Ω 30 pF	15	XFM-9S01	3.3 kΩ 2 pF	14
XF-9E	FM	XFM-9E	1.2 kΩ 30 pF	15	XFM-9S05	8.2 kΩ 0 pF	14
XF-9B01	LSB	XFM-9B01	500 Ω 30 pF	15	XFM-9S06	1.8 kΩ 3 pF	14
XF-9B02	USB	XFM-9B02	500 Ω 30 pF	15	XFM-9S07	1.8 kΩ 3 pF	14
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